Size-Dependent-Transport Study of $In_{0.53}Ga_{0.47}As$ Gate-All-Around Nanowire MOSFETs: Impact of Quantum Confinement and Volume Inversion

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***Abstract*—InGaAs gate-all-around nanowire MOSFETs with channel length down to 50 nm have been experimentally demonstrated by a top-down approach. The nanowire size-dependent transport properties have been systematically investigated. It is found that reducing nanowire dimension leads to higher on-current, transconductance, and effective mobility due to stronger quantum confinement and the volume-inversion effect. TCAD quantum mechanical simulation has been carried out to study the inversion charge distribution inside the nanowires. Volume-inversion effect appears at a larger dimension for InGaAs nanowire MOSFET than its Si counterpart.**

***Index Terms*—Gate-all-around (GAA), InGaAs, nanowire.**

I. Introduction

For beyond 14-nm logic applications, InGaAs MOSFETs have recently been considered as one of the promising candidates [1]. To meet the stringent demands of electrostatic control, nonplanar 3-D structures have been introduced to the fabrication of InGaAs MOSFETs, including InGaAs FinFETs [2], multigate InGaAs quantum-well FETs [3], and most recently, InGaAs gate-all-around (GAA) nanowire MOSFETs [4].

In particular, the InGaAs GAA nanowire MOSFETs have been shown to offer good scalability down to channel length (L_{ch}) of at least 50 nm, owing to the best electrostatic control of the GAA structure. High drive current (I_{on}) of 1.17 mA/μm and peak transconductance (g_m) of 0.7 mS/μm have also been achieved [4] despite the nonoptimized source/drain resistance (R_{SD}) and large equivalent oxide thickness (*EOT*), showing great promise of the InGaAs GAA technology. Moreover, a detailed scaling metrics study has also revealed that reducing the nanowire size leads to improvements in subthreshold swing *(SS)*, drain-induced barrier lowering (*DIBL*), and threshold voltage (V_T) rolloff, due to the tighter gate control [4]. However, the impact of nanowire size on the transport properties of InGaAs GAA nanowire MOSFETs has not been studied and could lead to better understanding and design guidelines for next-generation InGaAs nanowire devices.

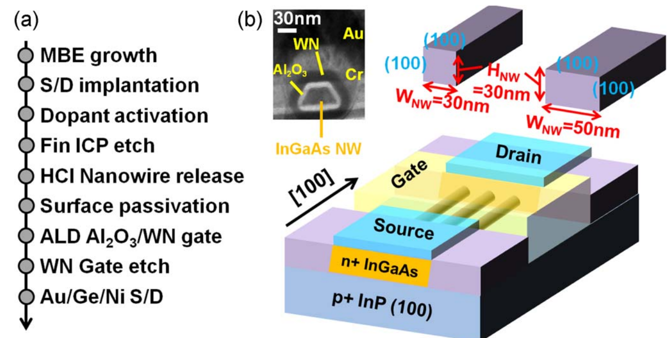

Fig. 1. (a) Key fabrication-process steps of InGaAs GAA nanowire MOSFETs by top-down approach. (b) Schematic diagram of an InGaAs GAA nanowire MOSFET and InGaAs nanowires with two different sizes under investigation (30 nm × 30 nm and 50 nm × 30 nm). Surface orientations (100) of the top surface and ideal side surface with vertical sidewall are illustrated. The nanowire patterning and current transport direction of [100] are depicted. A cross-sectional TEM image of an InGaAs GAA nanowire MOSFET with W_{NW} of 30 nm is also shown. The actual width and height of the nanowire are measured to be 26 and 27 nm with an $\sim 25^\circ$ angle between the actual and ideal sidewalls. Note that nanowires with vertical sidewall and designed W_{NW} are assumed in the normalization and simulation in this letter.

In this letter, we systematically investigate the impact of nanowire size on the ON-state performance of InGaAs GAA nanowire MOSFETs. To our surprise, higher I_{on} and intrinsic g_m have been obtained on devices with smaller nanowire size. The low field mobility (μ_0) is extracted using the Y-function method to further elucidate the transport performance of the nanowire devices [5], confirming the enhanced mobility for smaller nanowires. TCAD quantum mechanical simulation is employed to study the underlying physical mechanism [6]. It is shown that quantum confinement and volume-inversion effect play an important role in the improved transport properties for the InGaAs GAA nanowire MOSFETs.

II. Device Fabrication

Fig. 1 shows the fabrication-process flow as well as the schematic diagram of the InGaAs GAA nanowire MOSFET. The fabrication started with a 30-nm $In_{0.53}Ga_{0.47}As$ channel layer with a p-type doping of 2×10^{16} cm^{-3} epitaxially grown on a heavily p-doped InP (100) substrate by molecular

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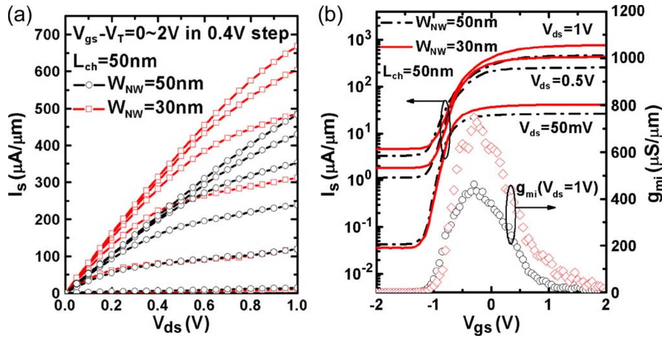

Fig. 2. (a) Output characteristics and (b) transfer characteristics and intrinsic g_m versus $V_{\rm gs}$ of two typical InGaAs GAA nanowire MOSFETs with $L_{\rm ch} = 50$ nm and (red) $W_{\rm NW} = 30$ and (black) 50 nm. I_s is used due to relatively large junction leakage current.

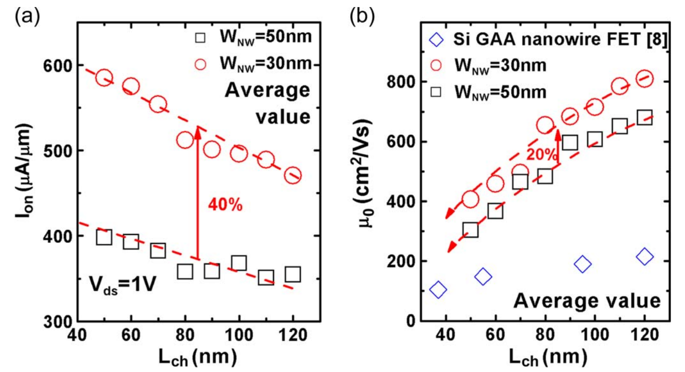

Fig. 3. Average value of (a) $I_{\rm on}$ measured at $V_{\rm gs} - V_T = 2$ V and $V_{\rm ds} = 1$ V and (b) low field mobility μ_0 of InGaAs GAA nanowire MOSFETs extracted using the Y-function method with $L_{\rm ch}$ varying from 50 to 120 nm and $W_{\rm NW}$'s of (red circle) 30 and (black square) 50 nm, compared to (diamond) Si GAA nanowire nMOSFET data [8]. Over 20 devices were measured at each data point to obtain the average value.

beam epitaxy (MBE). After source/drain implantation (Si, 1×10^{14} cm^{-2}, 20 keV), fin patterning was performed using BCl_3/Ar inductively coupled plasma (ICP) etching, followed by hydrogen chloride (HCl)-based nanowire-release process. The nanowires were aligned along [100] direction as required by the anisotropic HCl wet etching. After surface passivation with ammonia sulfide, 10-nm Al_2O_3 and 20-nm WN were grown by atomic layer deposition (ALD) at temperatures of 300 °C and 385 °C, respectively. Due to the excellent conformal coating ability of ALD, the gate stack forms surrounding all facets of the nanowires. Gate etch using CF_4-based ICP etching was then carried out to define the gate pattern. Finally, ohmic contacts were formed by electron beam evaporation of Au/Ge/Ni and liftoff process. Details of the fabrication process can be found in [4].

The fabricated devices have nominal $L_{\rm ch}$ varying from 120 down to 50 nm. Two different nanowire widths ($W_{\rm NW}$'s) (50 and 30 nm) were defined by lithography with a fixed nanowire height $(H_{\rm NW})$ of 30 nm defined by the MBE channel thickness. Since the nanowires were aligned along [100] direction, both the top and side surfaces are (100) surfaces assuming vertical sidewalls. Due to the nonoptimized fin-etching process, the actual sidewall leans 10°–30° toward (110) surface, confirmed by the SEM images [4].

III. Results and Discussion

Fig. 2(a) shows the output characteristics of two InGaAs GAA nanowire MOSFETs with $L_{\rm ch}$ of 50 nm. Devices with $W_{\rm NW}$'s of 30 and 50 nm exhibit saturation currents of 668 and 482 μA/μm at $V_{\rm gs} - V_T = 2$ V and $V_{\rm ds} = 1$ V, respectively. The current is normalized by the total *perimeter* of the nanowires. The device with smaller nanowire size has a 38% higher $I_{\rm on}$. Similar enhancement in intrinsic g_m is also observed on the smaller nanowire device as shown in Fig. 2(b). The V_T's of the devices with $W_{\rm NW}$'s of 30 and 50 nm are -0.85 and -0.94 V, respectively, from linear extrapolation at $V_{\rm ds} = 50$ mV. The negative V_T is due to the low work function of WN ($\sim$4.6 eV). Both devices show good pinchoff characteristics with an *SS* of 150 mV/dec at a $V_{\rm ds}$ of 50 mV. The upper limit of the interface trap density $(D_{\rm it})$ at midgap is estimated to be 5.6×10^{12} cm$^{-2} \cdot$ eV^{-1}. The device with $W_{\rm NW} = 30$ nm shows lower *DIBL* ($\sim$180 mV/V) compared to the device with $W_{\rm NW} = 50$ nm ($\sim$250 mV/V), indicating improved control of short-channel effects by shrinking the nanowire size. Considering the *EOT* of $\sim$4.5 nm and scaled $L_{\rm ch}$ of 50 nm, the *SS* and *DIBL* have been significantly improved compared to previous FinFET work [2], indicating the suitability of GAA structure for logic applications.

Fig. 3(a) shows the average $I_{\rm on}$ measured at $V_{\rm gs} - V_T = 2$ V and $V_{\rm ds} = 1$ V as a function of $L_{\rm ch}$. A gradual increase of $I_{\rm on}$ is observed when scaling down the channel length for both nanowire sizes. An average of 40% increase in $I_{\rm on}$ has been obtained on devices with $W_{\rm NW}$ of 30 nm over the entire $L_{\rm ch}$ range. Devices with different $W_{\rm NW}$'s show similar $R_{\rm SD}$, ranging from 950 to 1150 $\Omega \cdot \mu$m. The intrinsic g_m of devices with smaller nanowire size is found to be 34% higher than those with larger nanowire size (not shown). To further characterize the transport in the nanowire devices, effective mobility was extracted using the Y-function method, which agrees reasonably well with the split-CV method and allows for the suppression of the series-resistance effect [5]. Fig. 3(b) shows the average μ_0 versus $L_{\rm ch}$, demonstrating over 20% mobility enhancement for devices with smaller $W_{\rm NW}$. The apparent mobility reduction at shorter $L_{\rm ch}$ can be explained by Shur's model using a Matthiessen-like relation considering the ballistic mobility [7]. It is also shown in Fig. 3(b) that the extracted μ_0 of the InGaAs GAA nanowire MOSFETs is two to four times higher than those from state-of-the-art Si nanowire devices [8], owing to the better transport properties of the III–V channel.

The increase in $I_{\rm on}$, g_m, and μ_0 has confirmed that improved transport has been obtained in smaller InGaAs nanowires. Normally, for top-down nanowires, it is expected that reducing the nanowire size will degrade transport due to the relative increase in surface-roughness scattering given the larger surface-to-volume ratio of the ultrasmall nanowires. However, it has been reported on Si nanowire MOSFETs that the improved transport from high-mobility sidewall [9], oxidation-induced strain inside the nanowire [10], and the volume-inversion effect in nanowires with small cross-sectional area [11] would result in enhanced transport properties with $W_{\rm NW}$ shrinkage. The InGaAs (111)A surface has been demonstrated to offer higher mobility than other crystal orientations due to the trap redistribution [12]. However, the (111)A surface cannot be the sidewall facet of InGaAs nanowires in this study, since the nanowires are aligned

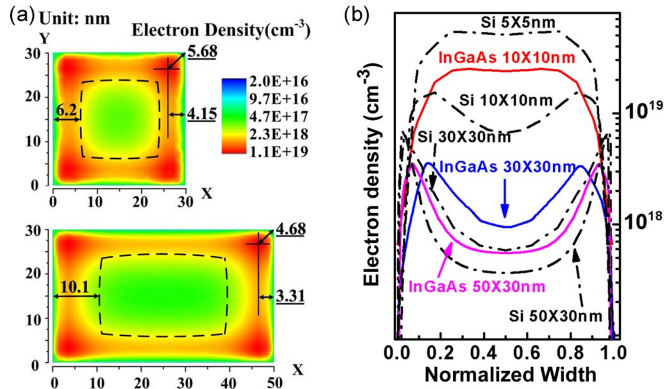

Fig. 4. (a) Cross-sectional distribution of electron density in the $\mathrm{In}_{0.53}\mathrm{Ga}_{0.47}$As nanowire with W_{NW}'s of 30 and 50 nm at $V_{\mathrm{gs}} - V_T =$ 1.2 V. Dashed line shows the inversion-layer centroid. (b) Normalized electron distribution at the middle of the nanowire $(y = 0.5H_{\mathrm{NW}})$ for square-shape Si and $\mathrm{In}_{0.53}\mathrm{Ga}_{0.47}$As nanowires. Note that vertical sidewalls are assumed in the simulation. While the sidewalls in the experiments are not vertical, resulting in reduced gate control, the general scaling trend comparing nanowires with different sizes remains unchanged.

along [100] direction. Moreover, the thermal budget of the fabrication process after nanowire release in this letter is as low as 385 °C, which is much lower than the thermal oxidation temperature (usually over 1000 °C) of the Si nanowire MOSFET [10]. Therefore, strain-induced mobility enhancement cannot play a significant role in the InGaAs nanowires under investigation. On the other hand, due to the much smaller effective mass and density of states of InGaAs, the inversion-layer thickness can be 3.5 times larger than that of Si. As a result, inversion carriers can be pushed further away from the interfaces due to a stronger quantum confinement leading to the volume-inversion effect in InGaAs nanowires at larger dimensions than Si.

To further clarify the underlying mechanism, TCAD simulation using Sentaurus Device [6] was carried out. The electron distribution inside the nanowire in the strong inversion regime is obtained using a coupled Poisson and quantum potential solver based on the density-gradient model [6], [13], considering only Γ valley for InGaAs. It is found that both InGaAs GAA nanowire MOSFETs with W_{NW}'s of 30 and 50 nm operate in the volume-inversion regime, where the inversion charge density inside the entire nanowire is higher than the background p-type doping. The $W_{\mathrm{NW}} = 30$ nm device shows stronger confinement, resulting in the inversion layer being pushed 1–2 nm further away from the surface and a higher inversion charge density at the center of the nanowire compared to the $W_{\mathrm{NW}} = 50$ nm case, as shown in Fig. 4(a). This would lead to suppressed surface-roughness scattering for the smaller nanowire. Furthermore, the volume inversion also results in the inversion-layer centroid of the smaller nanowire being closer to the surface and, therefore, an increase in electrostatic capacitance with decreasing W_{NW}. It is also found that the two inversion layers inside InGaAs nanowire would merge into one peak at a dimension of $\sim$10 nm, twice as large as that in the Si case ($\sim$5 nm) as shown in Fig. 4(b). The inversion layer distributes further inside the InGaAs nanowire with a higher density at the center compared to the Si case with the same nanowire size. Further experimental efforts reducing InGaAs nanowire size are required to illuminate on the ultimate scaling limit of InGaAs GAA nanowire MOSFETs, which may require development of new nanowire-thinning techniques. The volume inversion at a larger dimension and a stronger quantum confinement in the InGaAs GAA nanowire MOSFETs may relax the fabrication complexity and interface quality requirements for InGaAs nanowire devices.

IV. Conclusion

In this letter, we have fabricated and characterized InGaAs GAA nanowire MOSFETs with different nanowire sizes. Enhanced transport properties have been confirmed on InGaAs nanowires with a smaller dimension, due to a stronger quantum confinement and volume-inversion effect. It is shown that distribution of inversion carriers moves further away from the surface and volume inversion occurs at a larger dimension on InGaAs nanowire than its Si counterpart, making InGaAs GAA MOSFETs favorable for future logic applications.

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