Degradation of III-V inversion-type enhancement-mode MOSFETs

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***Abstract*—We performed gate ramp voltage stress on III-V InGaAs based MOSFETs. Stress induces trapped charge and it also leads to interface trap generation, which has detrimental effects on the subthreshold slope and on the transconductance. At high electric fields, before the hard breakdown, a very low-frequency high-current random telegraph noise appears at the gate, which seems to be not correlated with the soft breakdowns commonly observed in other devices.**

Keywords-stress; III-V MOSFET; reliability.

I. INTRODUCTION

In the past, III-V based MOSFETs have been evaluated as possible replacement for silicon N-MOSFETs in high speed VLSI-ULSI devices, which will face several scaling limits in the next decade [1-3]. One of the main limits of high speed VLSI-ULSI devices is the dynamic power dissipation, which depends on the square of the power supply voltage. From this viewpoint, III-V MOSFETs are very promising due to their much higher electron mobility with respect their silicon counterparts, which, in turn, translates in a much lower ON-state MOSFET resistance. Therefore, III-V MOSFETs allow to use much lower power supply voltages, while operating at the same switching speeds of their silicon counterpart, reducing the dynamic power consumption.

However, several issues affected III-V MOSFETs in the past, mainly due to the lack of a good gate dielectric. The native oxide forms a very poor semiconductor/dielectric interface, with an interface trap density so high that induces the pinning of the Fermi level, leading to very poor electrical characteristics [4-11]. Therefore, extensive research (see for instance [12-25]) was carried out to find materials and deposition techniques, which allowed the Fermi level unpinning.

This work was partially supported by Progetto di Ateneo 2009 – Università di Padova, Italy (Project Number CPDA083941).
The work at Purdue University is supported by United States National Science Foundation and the SRC FCRP MSD Center.

Recently, several advancements have been achieved both in flatband and inversion mode III-V MOSFETs, reaching electron mobility exceeding 5000 $cm^2V^{-1}s^{-1}$ [17,26,27].

Despite these improvements, III-V MOSFETs have still many open issues, such as very exacerbated short channel effects [28], which negatively impact on the static power consumption. Moreover, the reliability of III-V MOSFETs is still an unexplored field. In this work, we show the results of gate ramp stress performed on InGaAs inversion-type enhancement-mode MOSFETs.

This is the first reliability investigation on InGaAs MOSFET devices. Even if some preliminary reliability data on GaAs devices, have been recently published in [29], this study indeed represent the first deep and systematic investigation of the reliability of III-V MOSFETs devices.

This work is organized as follows: in Section II we describe the devices and the experimental procedure; in Section III-A we show and discuss the gate current stress kinetics; in Section III-B we discuss the impact on the electrical characteristics and the degradation kinetics on the extrapolated parameters; finally,

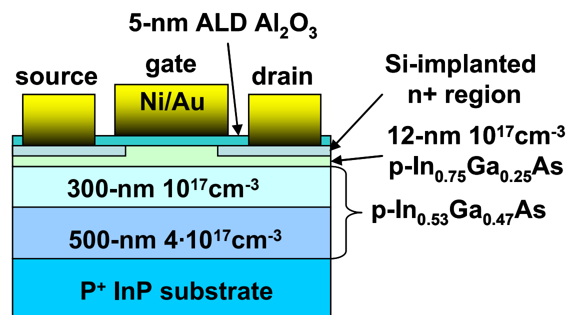

Figure 1. Cross section of the devices used throughout this work.

in Section IV we draw our conclusions.

II. Experimental and Devices

Throughout this work, we analyzed inversion-type enhancement-mode InGaAs with Al_2O_3 gate dielectric. Fig. 1 shows a schematic cross section of the analyzed devices. A 500-nm p-type $4\times10^{17}/cm^3$ buffer layer, a 300-nm p-type $1\times10^{17}/cm^3$ $In_{0.53}Ga_{0.47}As$ layer, and a 12-nm strained p-type $1\times10^{17}/cm^3$ $In_{0.75}Ga_{0.25}As$ channel were sequentially grown by molecular beam epitaxy over a p^+-InP substrate. The devices feature a 5-nm Al_2O_3 gate oxide. For further details, the interested reader may refer to [28]. The gate lengths (L) considered in this work were 150nm, 200nm, and 250nm. All the MOSFETs feature the same channel width W=5µm.

We performed gate ramp stress on devices with different channel lengths. The stress procedure is schematically depicted in Fig. 2a. The devices were initially characterized and they were subjected to a stress-characterization-relax-characterization loop, which lasted until device breakdown was detected. Each stress step consists of a 100-s constant voltage gate stress (CVS), with the other terminals grounded. The 200-s relax phase was introduced to neutralize any positive unstably trapped charge, which may affect the first characterization performed after each stress step, especially at the earlier stress steps (i.e. when the device is subjected to the lower stress voltages). During the relax phase, the gate was biased to -0.5V, while the other terminals were grounded.

Incidentally, in our samples, the drain to substrate diode features a quite large leakage, regardless the channel length. This leakage is drain voltage dependent and it is in the nA range even at V_{DB} as low as 0.2V. This current is quite high and it would not allow to appreciate the small variations, which occur at the very first stress steps, therefore, we extrapolated all our parameters from the source current, rather than drain current. Performance evaluation is outside the scope of this work, while our primary focus is to evaluate the stress impact and the degradation kinetics.

III. Results and Discussions

A. Gate current stress kinetics

In Fig. 3 we plot the gate current evolution measured during the stress, on devices with different L. Each stress step was followed by a relax phase (as in Fig. 2a). Noticeably, the kinetics are almost identical, regardless the L value. Remarkably, the gate current evolution of Fig. 3 can be divided in three distinct zones. In Zone 1 (V_{STRESS}<2.6V-2.8V), the gate current decreases during each step (Fig 4a). In Zone 2, (i.e. for 2.6V-2.8V<V_{STRESS}<3.6V-3.8V) the current increases during each step (Fig 4b). Zone 3 is characterized by soft and hard breakdowns (Fig. 4c).

The decreasing gate current evolution of each stress step in Zone 1 (see Fig. 4a) suggests the presence of bulk traps in the Al_2O_3 oxide, as also found in [30]. Since the trap density is finite, the gate current diminishes with time as the traps release their electrons, which then move toward the gate. Noticeably, those traps show a very slow response time. In fact, from Fig 4a, we argue that the response time of these traps is in the order of tens of seconds.

When the stress voltage is higher than 2.6V-2.8V (Zone 2), the gate current evolution starts to be increasing during each stress step (see Fig. 4b). This suggests that the increase of the gate current due to the formation of neutral traps in the dielectric dominates over the current relaxation observed in Fig. 4a.

Zone 3 (see Fig. 4c) features a very low frequency Random Telegraph Noise (RTN)-like evolution at rather high current values. It is well-known [31-33] that stressed oxides may feature gate leakage currents, which may be characterized by RTN. Still, in the literature, the RTN is observed at current

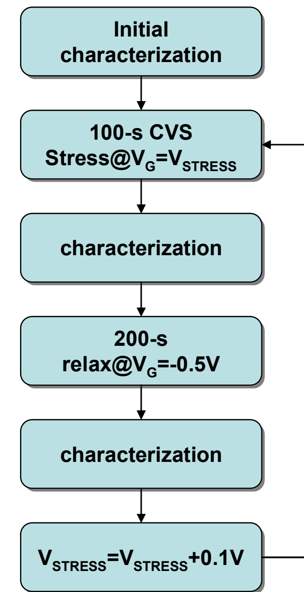

Figure 2. Experimental procedure adopted for the ramp stress with relax phase.

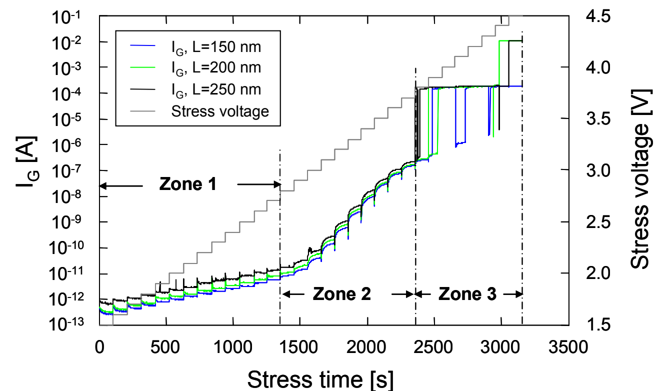

Figure 3. Evolution of the gate current measured during the stress. The stress kinetics has been divided in 3 zones featuring different behaviors (see zooms in Fig. 4).

values within the 1pA-100nA range, which are several orders of magnitude below the 100-μA range shown in Fig. 4c. Furthermore, it has been observed that the stronger the electric field, the higher is the RTN frequency [33], due to the onset of multilevel fluctuations induced by several separated leakage paths, while Fig. 4c (and the third zone of Fig. 3) has timescales in the 10-50s range and very high electric fields (exceeding 7MV/cm).

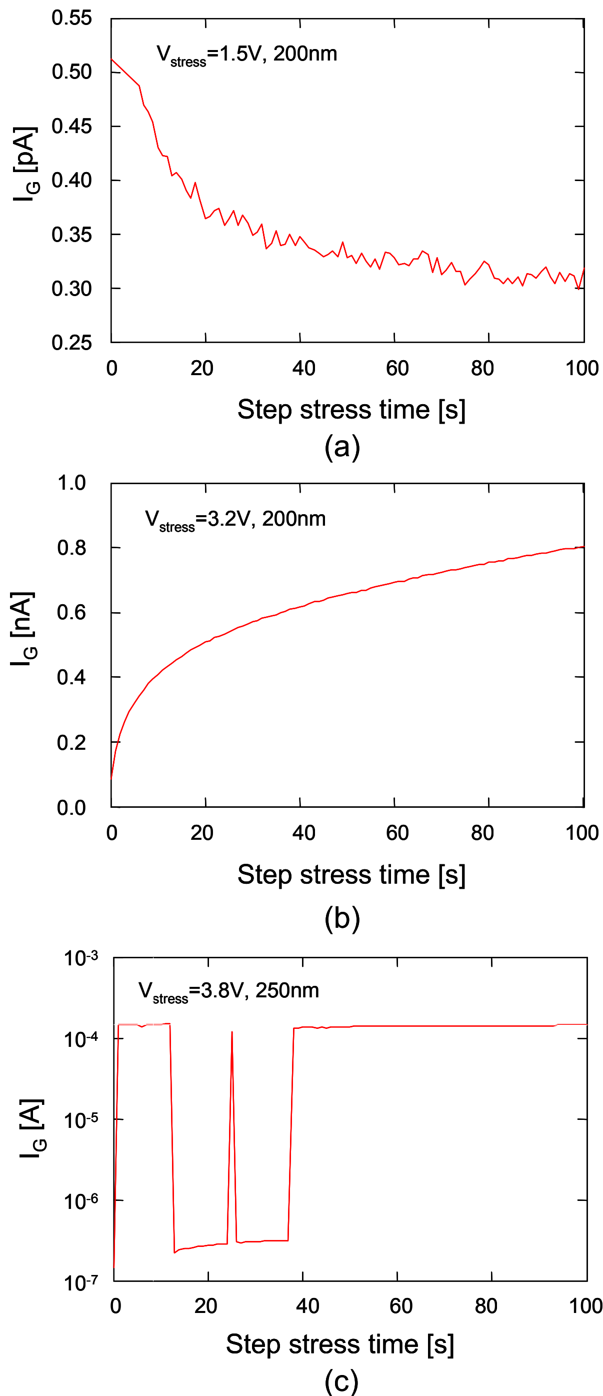

Figure 4. Zoom of 3 steps belonging to Zone 1 (a), Zone 2 (b) and Zone 3 (c) of Fig. 3.

Tentatively, we may attribute these low-frequency high-current fluctuations to the formation/rupture of a filament due to the high electric field, during the stress. The phenomenon is similar to what commonly happens in resistive random access memories, which works on the ability of some oxides (also Al_2O_3, see [34]) to reversibly switch their conductivity. The filament is generated by the very high gate electric fields and it induces a very high localized current flow, resulting in a local increase of the temperature. The high temperature may induce either a thermal runaway process, which further increases the gate current (hard breakdown), or it may lead to the filament rupture due to thermal redox and/or anodization [35]. Once the filament has been broken off, the gate current temporarily returns to a much smaller value, until the filament is opened again. The continuous random formation/rupture of the filament might be the responsible of the observed RTN-like I_G.

B. *Effects on the I-V characteristics and degradation kinetics*

In Fig. 5 we plot the I_S-V_{GS} and I_G-V_{GS} taken after various stress steps on a 250-nm gate-length device. Remarkably, the gate current (see Fig. 5b) features a noticeable permanent increase only for V_{STRESS}>3.5V indicating that an Al_2O_3 electric field larger than ~6.5MV/cm (value calculated taking into account the flatband voltage and the semiconductor band bending) is required to appreciably degrade the gate dielectric, at least within 100s. Noticeably, this threshold V_{STRESS} value matches the gate-to-bulk voltage required to achieve Fowler-Nordheim (FN) Injection of electrons, which could enhance the dielectric degradation. Breakdown occurs at Al_2O_3 electric fields larger than ~7MV/cm, which is a value that is in good agreement with data reported in other works [36-37] for Al_2O_3.

In Figs 6-13 we plot the evolution of some of the most important MOSFET parameters during the electrical stress. The degradation kinetics is shown as a function of the applied gate voltages. All curves refer to the characteristics measured after the relax phase. In particular, we show the subthreshold slope (SS), the ON current (I_{ON}, measured with V_{DS}=V_{GS}=1V), the leakage current at V_{GS}=-0.5V and V_{DS}=1V, the transconductance peak, and the threshold voltage (V_{th}). V_{th} has

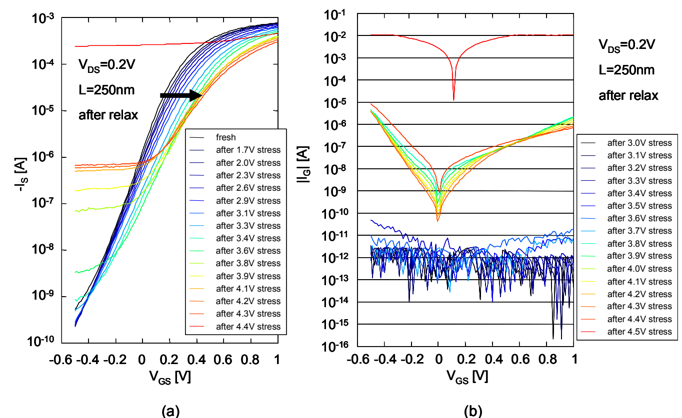

Figure 5. (a) Source-current- and gate-current- (b) gate-to-source-voltage-characteristics measured on a device with L=250nm, after each stress step, after relax.

been defined as the V_{GS} required to drive a drain current chosen so that $L \cdot I_D$ equals to 0.5 A·cm, to take into account the different W/L values.

Noticeably, the subthreshold slope increases with the stress voltage, (Fig. 6) indicating that new semiconductor/dielectric interface traps are generated. The transconductance peak (Fig 7) and, consequently, I_{ON} (Fig 8), are both decreasing, with increasing stress voltage. Incidentally, there is an almost linear correlation between the inverse of the transconductance peak, normalized to its fresh value, and the subthreshold slope, normalized to its fresh value (Fig. 9). This suggests that the transconductance variation is due to the mobility degradation, which, in turn, is affected by the interface trap generation as widely confirmed in the literature (see for instance [38]).

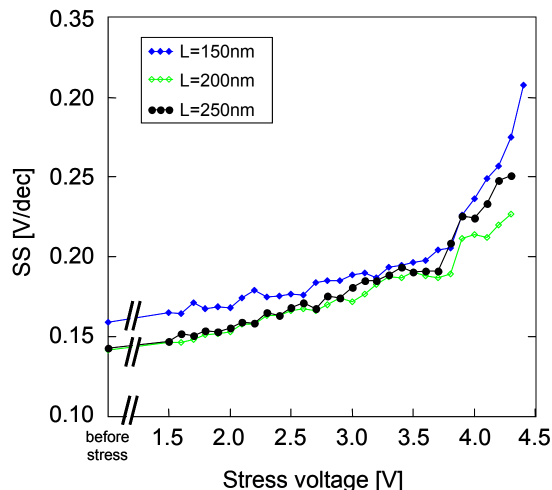

Figure 6. Subthreshold slope extrapolated from the characterizations performed after the relax phases.

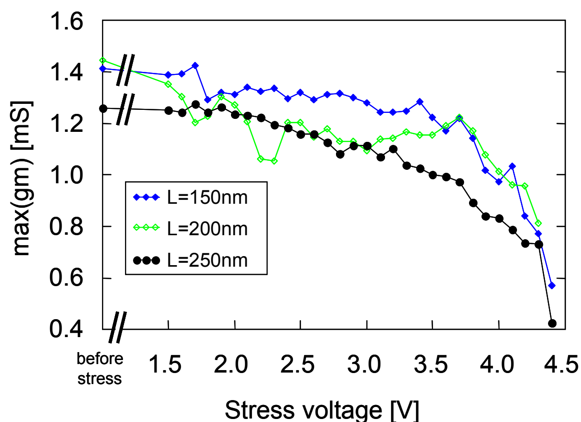

Figure 7. Transconductance peak extrapolated from the characterizations performed after the relax phases. V_{DS}=0.2V.

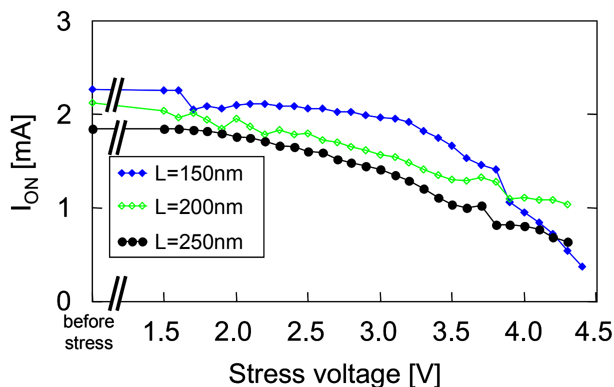

Figure 8. ON-state source current, measured at V_{DS}=V_{GS}=1V after each relax phase.

Remarkably there is also an increase of the leakage current (Fig. 10) especially at the latter stress steps. The observation of the drain- (Fig. 11a), source- (Fig. 5a), bulk- (Fig 11b) and gate- (Fig. 5b) currents as a function of the gate voltage leads to the conclusion that the observed leakage current (measured at V_{GS}<0V) is a true drain-to-source current (i.e. it is a current flowing through the channel).

We ascribe the increased drain-to source leakage to two

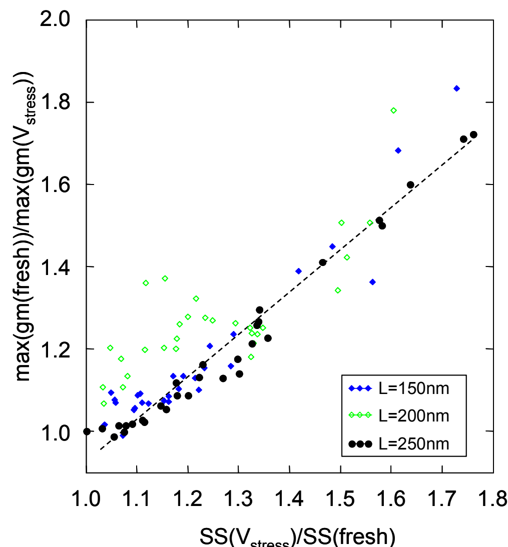

Figure 9. Correlation between the subthreshold slope (normalized to its pre-stress value) and the inverse of the transconductance peak (normalized to its pre-stress value).

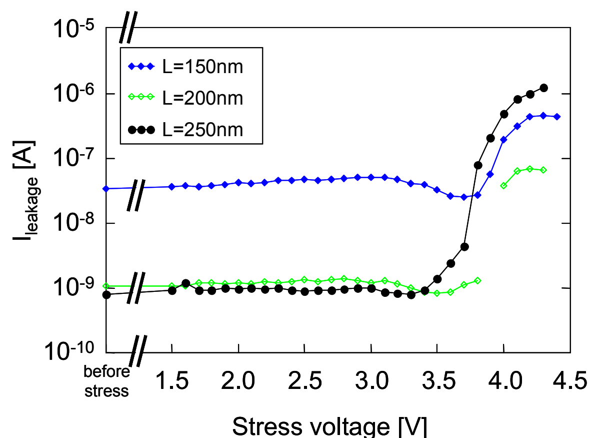

Figure 10. Source leakage current, measured at V_{DS}=1V, V_{GS}=-0.5V after each relax phase.

phenomena. First, positive charges might be trapped near the edges of the gate, where the electric fields are enhanced during stress by the sharp shape of the gate edges. The positive trapped charge in the Al_2O_3 near the gate edges might then induce a parasitic low-V_{TH} lateral MOSFET, increasing the drain-to-source leakage current. Noticeably, our devices do not feature any field or shallow trench isolation.

The second possible explanation for the onset of the drain-to-source current could be the Fermi level pinning at the channel surface, induced by the stress-induced additional interface traps. In fact, the observed leakage current is almost independent of V_{GS} (see Fig. 5a and Fig 11a). This conclusion is consistent to [39], where the minimum OFF-state leakage current on inversion-type III-V MOSFET was ascribed to the Fermi level pinning at the channel surface. The combined effects of Fermi level pinning and the parasitic lateral MOSFET might be the root cause for the strong increase of the drain-to-source leakage current measured for $V_{GS}<0$.

At this point, one might also wonder if the observed increased leakage current is indeed a drain-to-source current or, if it derives from the increased drain-to-substrate and source-to-substrate leakage currents, due to a possible stress-induced drain and source junctions' degradation. However, analyzing the I-V characteristics measured after each relax phase, we found that:

F1) the leakage current increase at the source is equal to the leakage current increase measured at the drain, and this relation holds for each V_{DS} at which the I-V characteristics have been taken, i.e. up to 1V (please note that for sake of simplicity, in Figs. 5 and 11 we show only the I-V taken at V_{DS}=0.2V). Of course, the value of the source/drain leakage increase depends on the V_{DS}.

F2) The difference (i.e. the algebraic sum) between the source and drain currents, measured after each stress step, is almost equal to the drain-to-bulk leakage current measured before the device was subjected to any stress.

If the origin of the increased leakage at the source and drain were the stress-induced source and drain junctions' degradation, we would expect a very large leakage dependence on the applied bias (i.e. V_{DB} and V_{SB}). However, as we stated in F1, we found that the increase of the leakage current at the source (which has V_{SB}=0 ±100μV) is equal to the increase of the leakage current at the drain (which has V_{DB} from 0.2V up to 1V). Furthermore, F2 suggests that the drain-to-bulk leakage current is unaffected by the stress. In other words F2 suggests that is the junction is not degraded by the stress.

One might also hypothesize that the drain and source junctions were not equally degraded by the stress. However, in that case, F1, would not hold for every V_{DS}. Furthermore, our devices are geometrically symmetrical and, during the stress, the source and drain were at the same potential (0V), thus we expect an uniform degradation (if any) at the source and drain junctions.

The comparison of Fig. 5b and Fig. 11b gives us also some information about the position of the soft breakdown. As expected, the breakdown is not preferably located near the drain or the source (because of the uniform stress setup, i.e. with V_B=V_S=V_D), and it manifests itself as a gate to bulk current, as confirmed by the diode-like I-V characteristics shown in Fig. 12b for V_{STRESS}≥3.8V.

Finally, V_{th} increases with increasing stress voltage as shown in Fig. 12. The increase of V_{th} arises from many contributions:

1) the subthreshold slope increase;

2) the reduction of the transconductance;

3) the negative charge trapping.

To assess how much charge has been trapped in the

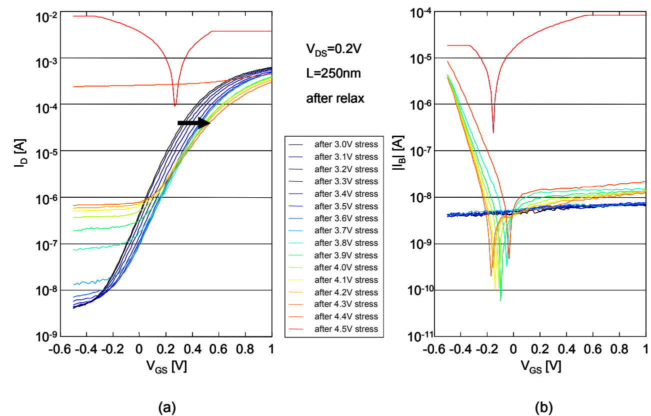

Figure 11. (a) Drain-current- and bulk-current- (b) gate-to-source-voltage characteristics measured on a device with L=250nm, after each stress step, after relax.

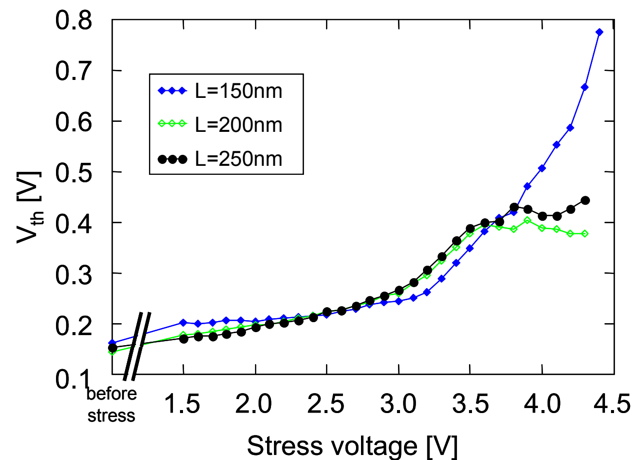

Figure 12. Threshold voltage extrapolated from the characterizations performed after the relax phases. V_{DS}=0.2V.

dielectric, we evaluated the midgap voltage variation using the well known subthreshold-midgap method [40-41]. The midgap voltage of fresh devices has been calculated analytically and it has been estimated to 45mV. In Fig. 13, we show the midgap voltage variation and the corresponding estimated dielectric trapped charge, as if it were concentrated in the center of the dielectric. Noticeably, the midgap voltage variation is smaller than V_{th}. The trapped charge at breakdown may vary between different samples, but it is within $3\sim9\cdot10^{12}$ electrons/cm^2.

IV. Conclusions

In this work we showed the results of gate ramp stresses performed on III-V inversion mode MOSFETs with different gate lengths. This is the first works that present systematic and deep investigation of electrical stress on InGaAs-based MOSFETs.

The interface trap generation reduces the ON-state current due to mobility and subthreshold slope degradation. Negative charge trapping also induces a threshold voltage increase, further reducing the ON-state current. Interface trap generation also may play a role in increasing the OFF-state leakage current, due to Fermi level pinning.

The increased OFF-state leakage current might be also induced by the onset of a parasitic lateral MOSFET due to positive charge trapping in the gate dielectric near the gate edges, where the electric field is locally enhanced.

A peculiar device soft breakdown is observed at Al_2O_3 electric fields around 7MV/cm. This soft breakdown is characterized by a very low-frequency RTN-like high gate current and it may be correlated to the continuous generation and rupture of a filament in the oxide as it happens in resistive memories.

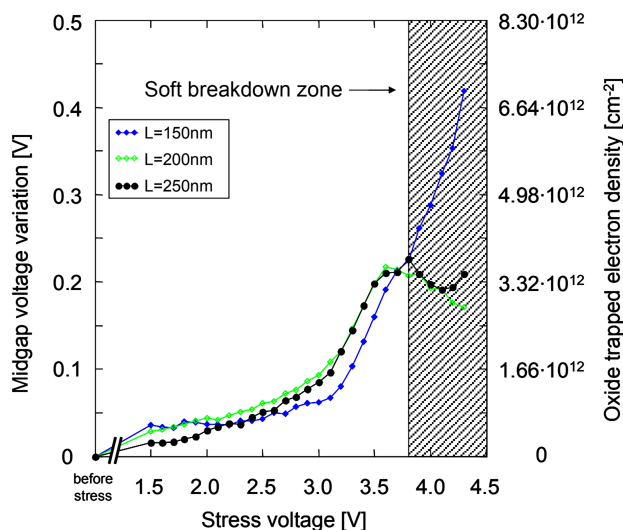

Figure 13. Evolution of the midgap voltage variation (left scale) and corresponding oxide trapped electron density variation induced by stress.

References

[1] R. Chau, S. Datta, and A. Majumdar, “Opportunities and challenges of III–V nanoelectronics for future high speed, low power logic applications,” in Proc. IEEE CSIC Tech. Dig., 2005, pp. 17–20.

[2] ‘Process integration, devices, and structures’ in ‘International technology roadmap for semiconductors’, 2007, ITRS. p. 3-4, www.itrs.net.

[3] Semiconductor Research Corporation website: www.src.org.

[4] H. Becke, R. Hall, and J. White, “Gallium arsenide MOS transistors,” Solid-State Electronics., vol. 8, pp. 813–823, 1965.

[5] T. Ito and Y. Sakai, “The GaAs inversion-type MIS transistors,” Solid-State Electronics., vol. 17, no. 7, pp. 751–759, 1974.

[6] B. Bayraktaroglu, E. Kohn, and H. L. Hartnagel, “First anodic-oxide GaAs M.O.S.F.E.T.S based on easy technological processes,” Electronics Lett., vol. 12, no. 2, pp. 53–54, 1976.

[7] A. Colquhoun, E. Kohn, and H. L. Hartnagel, “Improved enhancement/ depletion GaAs MOSFET using anodic oxide as the gate insulator,” IEEE Trans. Elec. Dev., vol. 25, pp. 375–376, Mar. 1978.

[8] T. Mimura, K. Odani, N. Yokoyama, and M. Fukuta, “New structure of enhancement-mode GaAs microwave M.O.S.F.E.T.,” Electron. Lett., vol. 14, no. 16, pp. 500–502, 1978.

[9] T. Mimura, K. Odani, N. Yokoyama, Y. Nakayama, and M. Fukuta, “GaAs microwave MOSFETs,” IEEE Trans. Elec. Dev., vol.25, pp. 573–579, June 1978.

[10] K. Kamimura and Y. Sakai, “The properties of GaAs–Al O and InP–Al O interfaces and the fabrication of MIS field-effect transistors,” Thin Solid Films, vol. 56, pp. 215–223, 1979.

[11] G. G. Fountain, R. A. Rudder, S. V. Hattangady, R. J. Markunas, and J. A. Hutchby, “Demonstration of an n-channel inversion mode GaAs MISFET,” in IEDM Tech. Dig., Dec. 1989, pp. 887–889.

[12] Y. C. Wang et al., “Advances in GaAs MOSFETs using Ga2O3 (Gd_2O_3) as gate oxide,” in Proc. Mater. Res. Soc. Symp., 1999, vol. 573, pp. 219–225.

[13] M. Passlack, J. K. Abrokwah, R. Droopad, Z.Yu, C. Overgaard, S. I.Yi, M. Hale, J. Sexton, and A. C. Kummel, “Self-aligned GaAs p-channel enhancement mode MOS heterostructure field-effect transistor,” IEEE Electron Device Lett., vol. 23, no. 9, pp. 508–510, Sep. 2002.

[14] M. Hale, S.I. Yi, J.Z. Sexton, A.C. Kummel, and M. Passlack, "Scanning Tunneling Microscopy and Spectroscopy of Gallium Oxide Deposition and Oxidation on GaAs(001)-c(2x8)/(2x4)", J. Chemical Physics, vol. 119, no. 13, pp.6719 -6728, 2003.

[15] Z. Yu, C. M. Overgaard, R. Droopad, M. Passlack, and J. K. Abrokwah, “Growth and physical properties of GaO thin films on GaAs(001) substrate by molecular-beam epitaxy,” Appl. Phys. Lett., vol. 82, no. 18, pp. 2978–2980, May 2003.

[16] M. Passlack, R. Droopad, K. Rajagopalan, J. Abrokwah, R. Gregory, D. Nguyen, "High Mobility NMOSFET Structure with High-K Dielectric," IEEE Electron. Dev. Lett., vol. 26, no. 10, pp. 713-715, 2005.

[17] R. Droopad, K. Rajagopalan, J. Abrokwah, M. Canonico, and M. Passlack, "Ino 75Gao 25As Channel Layers with Record Mobility Exceeding 12,000 cm^2/Vs for Use in High-K Dielectric NMOSFETs," Solid State Electronics, vol. 50, no.7-8, pp. 1175-1177, 2006.

[18] Y. Xuan, H. C. Lin, P. D. Ye, and G. D.Wilk, “Capacitance-voltage studies on enhancement-mode InGaAs metal-oxide-semiconductor field-effecttransistor using atomic-layer-deposited Al2O3 gate dielectric,” Appl. Phys. Lett., vol. 88, no. 26, pp. 263 518–263 520, Jun. 2006.

[19] K. Rajagopalan, J. Abrokwah, R. Droopad, and M. Passlack,“Enhancement-mode GaAs n-channel MOSFET,” IEEE Electron Devices Lett., vol. 27, no. 12, pp. 959–962, Dec. 2006.

[20] I. Ok et al., “Self-Aligned n- and p-channel GaAs MOSFETs on undoped and p-type substrates using HfO2 and silicon interface passivation layer,” in IEDM Tech. Dig., Dec. 2006, pp. 829–832.

[21] K. Rajagopalan et al., “1-μm enhancement mode GaAs n-channel MOSFETs with transconductance exceeding 250 mS/mm,” IEEE Electron Devices Lett., vol. 28, no. 2, pp. 100–102, Feb. 2007.

[22] Y. Sun et al., “Enhancement-mode buried-channel $In_{0.70}Ga_{0.30}As$/ $In_{0.52}Al_{0.48}As$ MOSFETs with high-k gate dielectrics,” IEEE Electron Devices Lett., vol. 28, no. 6, pp. 473–475, Jun. 2007.

[23] H. C. Lin et al., “Enhancement-mode GaAs metal-oxide-semiconductor high-electron-mobility transistors with atomic layer deposited Al_2O_3 as gate dielectric,” Appl. Phys. Lett., vol. 91, no. 21, pp. 212 101–212 103, Nov. 2007.

[24] Y. Xuan, Y. Q. Wu, H. C. Lin, T. Shen, and P. D. Ye, “Submicrometer inversion-type enhancement-mode InGaAs MOSFET with atomic-layerdeposited Al_2O_3 as gate dielectric,” IEEE Electron Devices Lett., vol. 28, no. 11, pp. 935–938, Nov. 2007.

[25] Y. Xuan, Y. Q. Wu, T. Shen, T. Yang, and P. D. Ye, “High performance submicron inversion-type enhancement-mode InGaAs MOSFETs with ALD Al_2O_3, HfO_2, HfAlO as gate dielectrics,” in IEDM Tech. Dig., Dec. 2007, pp. 637–640.

[26] M. Passlack, R. Droopad, K. Rajagopalan, J. Abrokwah, P. Zurcher; P. Fejes, "High Mobility III-V Mosfet Technology," . *IEEE Compound Semiconductor Integrated Circuit Symposium, 2006. CSIC 2006*, pp.39-42, Nov. 2006

[27] R.J.W. Hill, D.A.J. Moran, Li Xu, Zhou Haiping, D. Macintyre, S. Thoms, A. Asenov, P. Zurcher, K. Rajagopalan, J. Abrokwah, R. Droopad, M. Passlack, I.G. Thayne, "Enhancement-Mode GaAs MOSFETs With an $In_{0.3}$ $Ga_{0.7}As$ Channel, a Mobility of Over 5000 $cm^2/V \cdot s$, and Transconductance of Over 475 µS/µm," *IEEE Electron Device Letters,* vol.28, no.12, pp.1080-1082, Dec. 2007

[28] Y.Q. Wu, W.K. Wang, O. Koybasi, D.N. Zakharov, E.A. Stach, S. Nakahara, J. Hwang, P.D.Ye, "0.8-V Supply Voltage Deep-Submicrometer Inversion-Mode $In_{0.75}Ga_{0.25}As$ MOSFET," *IEEE Electron Device Letters,* vol.30, no.7, pp.700-702, July 2009.

[29] Z. Tang, P.D. Ye, D. Lee, C.R. Wie, "Electrical measurements of voltage stressed Al_2O_3/GaAs MOSFET" Microelectronics Reliability, vol 47, pp. 2082-2087, 2007.

[30] D. Varghese, Y. Xuan, Y. Q. Wu, T. Shen, P. D. Ye, and M. A. Alam "Multi-probe Interface Characterization of $In_{0.65}Ga_{0.35}As/Al_2O_3$ MOSFET", in IEDM Tech. Dig., Dec. 2008, pp 379-382.

[31] A. Cester, L. Bandiera, G. Ghidini, I. Bloom, And A. Paccagnella, “Soft Breakdown Current Noise in Ultra-thin Gate Oxides,” Solid-State Electronics, vol. 46, p. 1019-1025, 2002.

[32] T. Tomita, H. Utsunomiya, T. Sakura, Y. Kamakura and K. Taniguchi , A new soft breakdown model for thin thermal SiO_2 films under constant current stress. *IEEE Trans. Elec. Dev., vol* **46** no. 1, pp. 159–164, 1999.

[33] M. Depas, T. Nigam and M.M. Heyns , Soft breakdown of ultra-thin gate oxide layers. IEEE T Electron Dev 43 9 (1996), pp. 1499–1504.

[34] Chih-Yang Lin, Dai-Ying Lee, Sheng-Yi Wang, Chun-Chieh Lin, Tseung-Yuen Tseng, “Effect of thermal treatment on resistive switching characteristics in $Pt/Ti/Al_2O_3/Pt$ devices,” Surface & Coatings Technology 203 (2008) 628–631.

[35] Kyung Min Kim, Byung Joon Choi, and Cheol Seong Hwang, “Localized switching mechanism in resistive switching of atomic-layer-deposited TiO_2 thin films,” Appl. Phys. Lett. 90, 242906 2007.

[36] H. C. Lin, P. D. Ye, and G. D. Wilk,” Leakage current and breakdown electric-field studies on ultrathin atomic-layer-deposited Al_2O_3 on GaAs,” Appl. Phys. Lett. 87, 182904, 2005.

[37] M.D. Groner, J.W. Elam, F.H. Fabreguette, S.M. George, “Electrical characterization of thin Al_2O_3 films grownby atomic layer deposition on silicon and various metal substrates,” Thin Solid Films 413 (2002) 186–197.

[38] S. C. Sun and J. D. Plummer, "Electron Mobility in Inversion and Accumulation Layers on Thermally Oxidised Silicon Surfaces," IEEE Trans. Electron Dev. ED-27, 1497 (1980).

[39] M. Passlack, “OFF-State Current Limits of Narrow Bandgap MOSFETs,“ IEEE Trans. Elec. Dev., vol. 53, 2006, pp. 2773-2778.

[40] P. S. Winokur, J. R. Schwank, P. J. McWhorter, P. V. Dressendorfer, and D. C. Turpin, "Correlating the Radiation Response of MOS Capacitors and Transistors," IEEE Trans. Nuc. Sci. w, 1453 (1984).

[41] P. J. McWhorter and P. S. Winokur, "Simple Technique for Separating the Effects of Interface Traps and Trapped-Oxide Charge in Metal-Oxide-Semiconductor Transistors," Appl. Phys. Lett. 48, 133 (1986).