Characterization and Reliability of III-V Gate-all-around MOSFETs

Mengwei Si*, SangHoon Shin, Nathan J. Conrad, Jiangjiang Gu
Jingyun Zhang, Muhammad A. Alam, Peide D. Ye#

School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907, USA
Phone: 1-765-494-7611, Fax: 1-765-496-6443, Email: *msi@purdue.edu; #yep@purdue.edu

(Invited Paper)

***Abstract* – InGaAs is a promising channel material for high performance CMOS logic circuits due to its large electron injection velocity. InGaAs Gate-All-Around (GAA) MOSFETs have been demonstrated; these transistors offer large drive current and excellent immunity to short channel effects (SCE). However, the characterization and reliability of InGaAs GAA MOSFETs are still challenging. In this paper, we (i) discuss the challenges and new characterization methodologies to evaluate D_{it}, R_{sd} and other parameters on short channel InGaAs GAA MOSFETs, (ii) discuss device characterization based on low frequency noise and RTN, (iii) image the complexity of heat dissipation by using newly developed thermoreflectance method, and (iv) review the current research on 3D InGaAs MOSFET reliability including PBTI, HCI, and gate dielectric breakdown.**

[Keywords: InGaAs, Gate-all around nanowire MOSFET, Characterization, reliability, Thermoreflectance method]

I. Introduction

InGaAs has been considered as one of the promising channel materials for future CMOS logic circuit due to its large electron injection velocity [1]. 3D InGaAs MOSETs including FinFET, Multi-Gate FET, Gate-All-Around (GAA) MOSFETs have already been demonstrated. These transistors offer larger drive currents and excellent immunity to short channel effects (SCE) down to 20nm [2-10]. Further improvement and ultimate adoption of the GAA technology will depend on the ability to improve the interface and ensure 10-year device reliability.

Unfortunately, traditional D_{it} and effective mobility (μ_{eff}) extraction methods based on I-V measurements become a challenge because of the low density of states in InGaAs, the reduced gate to body capacitance (C_{GB}) and extremely short channel [11, 12]. Furthermore, conventional defect characterization methods on planar MOSFETs, such as C-V method and charge pumping method, become difficult due to the extremely small nanowire channel area and the suspended structure by design. As a result, noise, RTN and other non-capacitance based characterization techniques become alternative probes to characterize the property of short channel nanowire MOSFETs [13, 14]. Moreover, the unique structure

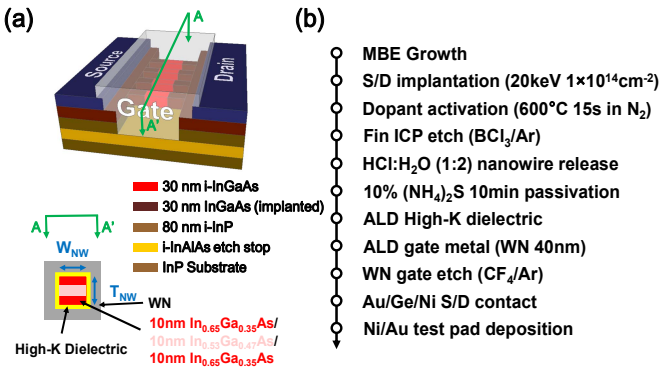

Fig. 1 (a) Schematic diagram, cross-sectional view and (b) fabrication process of an InGaAs GAA MOSFET.

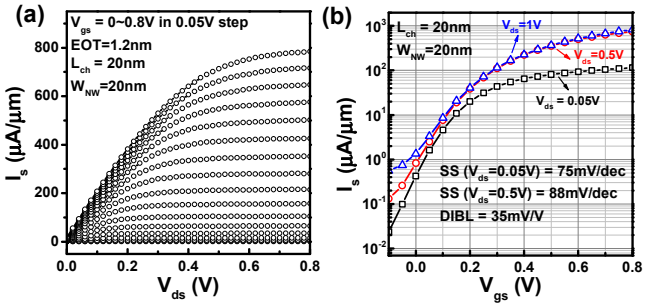

Fig. 2 (a) Output and (b) transfer characteristics of a 20nm L_{ch} GAA MOSFET with $Al_2O_3/LaAlO_3$ gate dielectric (EOT=1.2nm) and W_{NW}=20nm. I_s is used due to relatively large junction leakage current in I_d.

of InGaAs nanowire MOSFETs provide opportunities for new characterization methods but also new challenges.

Similarly, device reliability is very important for a manufacturable CMOS technology. Reliability performance of InGaAs MOSFETs have not met the criteria for massive production and unique reliability challenges on emerging III-V nanowire devices are also needed to be addressed [15-25]. Heat dissipation could also be a potential challenge, especially for GAA structures where the channel is surrounded by oxides and ALD-deposited gate metal, neither of which have high thermal conductivity. In this paper, we (i) discuss the challenges and methods to evaluate D_{it}, R_{sd} and other parameters on short channel InGaAs GAA MOSFETs, (ii) discuss device characterization based on low frequency noise

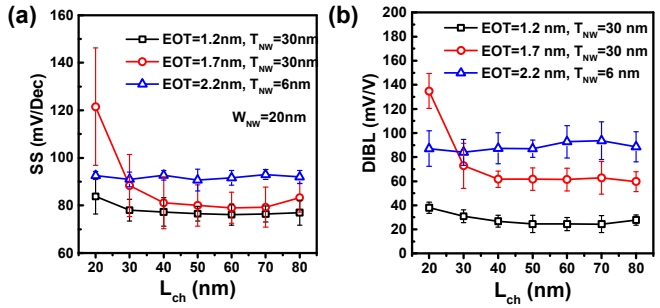

Fig. 3(a) SS and (b) DIBL channel length scaling metrics for different EOT and nanowire dimensions.

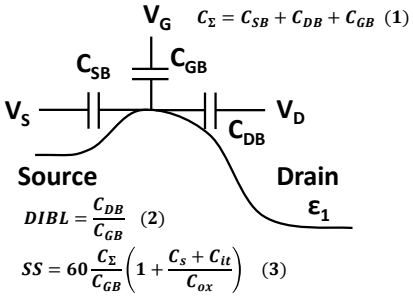

Fig. 4 Illustration of capacitance model on short channel devices. C_{SB}, C_{DB} and C_{GB} represent source to body capacitance, drain to body capacitance and gate to body capacitance respectively. ε_1 is the first subband of conduction band. The effect of C_{DB} on SS can be eliminated with measured DIBL which improves D_{it} extraction accuracy.

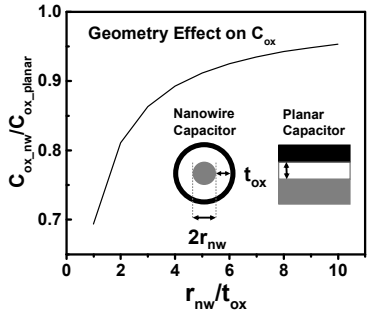

Fig. 5 Geometry effect of nanowire on C_{ox}. C_{ox} of nanowire MOSFET is lower compared to C_{ox} of planar MOSFET with the same t_{ox} due to the radiant electric field.

and RTN and (iii) analyze heat dissipation and the number of nanowire dependence by newly developed thermoreflectance method, (iv) review the current research on 3D InGaAs MOSFET reliability including PBTI, HCI, and failure analysis by thermoreflectance.

II. The General Performance of III-V GAA MOSFETs

A. Defect Characterization by DIBL-SS Correlation

The device structure and fabrication process of InGaAs GAA MOSFETs are shown in Fig. 1 and more detailed discussion can be found in [3]. Fig. 2 shows the well-behaved output and transfer characteristics of an L_{ch}=20nm nanowire device while SS and DIBL scaling metrics are shown in Fig. 3 with various nanowire dimensions and EOTs. The InGaAs nanowire devices show promising on-state and off-state performance with L_{ch} down to 20nm. However, to extract

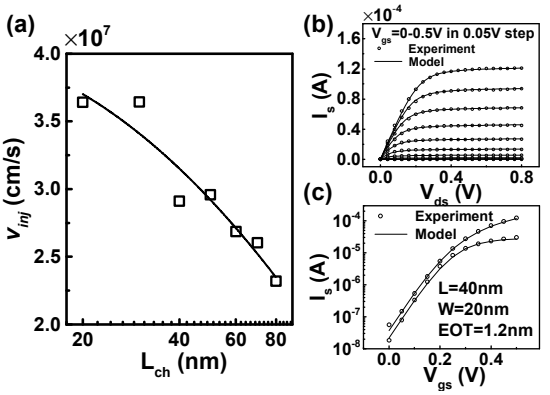

Fig. 6 (a) virtual source velocity extracted from Virtual Source Model. (b) and (c) comparison between model current (lines) and experimental data (circles).

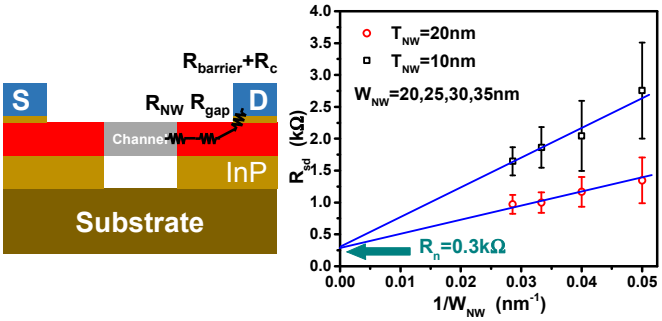

Fig. 7 Relation between series resistance R_{sd} and $1/W_{NW}$ of InGaAs GAA MOSFETs with 10 nm and 20 nm channel thickness. Each data point represents over 20 devices. R_{sd} can be divided into two parts. One is a function of W_{NW}, the other is non-related R_{gap}+$R_{barrier}$+R_c. By linear fitting, the non-related part can be extracted which reflects the resistance of contact and S/D sheet resistance.

physical parameters such as D_{it} and mobility becomes challenges. Firstly, the small nanowire gate area (~2×10^{-3} μm^2/wire) makes it hard to determine gate capacitance using C-V method. It's also difficult to apply charge pumping method due to the suspended channel and very small device interface area. Second, the strong SCEs and quantum confinement effects in devices with deeply scaled L_{ch} and nanowire cross section area make C_{GB} and C_{DB} (drain to body capacitance) comparable as illustrated in Fig. 4. Third, the C_{GB} of the devices cannot be calculated only from EOT. The low density of states, nanowire structure and quantum capacitance should also be taken into account. Careful simulation of C_{GB} might be a solution due to the difficulty in measurement. Taking the above three points into account, D_{it} extraction based on subthreshold (SS) method should be modified to eq. (3) in Fig. 4. By estimating DIBL=C_{DB}/C_{GB} from capacitor model of SCE [26], the effects of C_{DB} can be eliminated as shown in eq. (2-3) in Fig. 4. The other effect to be considered is the geometry effect on C_{ox}. A simple geometrical calculation on capacitance with same oxide thickness (t_{ox}) in cylinder nanowire and planar structure is different as shown in Fig. 5. C_{ox} in this work is about 80% of that calculated from ε_{ox}/t_{ox} with r_{nw}/t_{ox}=2. In short channel devices, current model deviates from conventional 1/L scaling and a semi-empirical virtual source model was developed to extract v_{inj} (carrier velocity at virtual source) by fitting method [27]. By applying this model to InGaAs GAA devices, the v_{inj} is extracted in Fig. 6(a), v_{inj} is ~3 times higher compared to Si

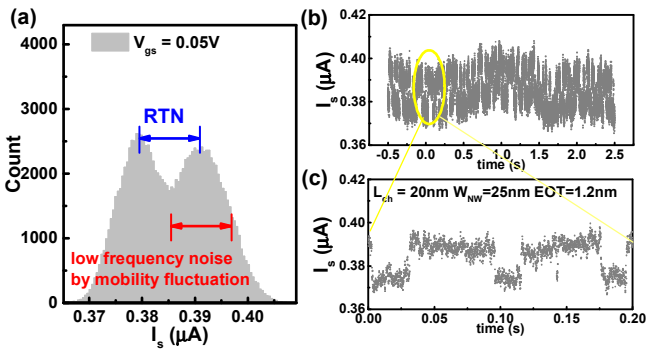

Fig. 8 (a) Histogram of a RTN signal of a device with L_{ch}=20nm and W_{NW}=25nm and EOT=1.2nm. (b) and (c) RTN signals in time domain of the same signal as (a). (c) is a time segment inside (b).

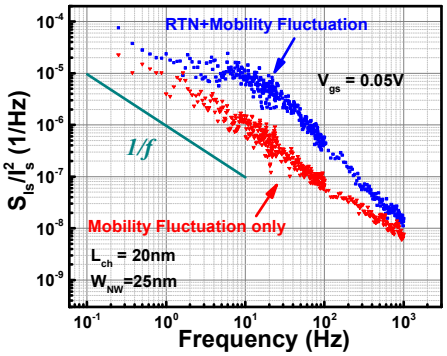

Fig. 9 Normalized I_s noise of devices (L_{ch}=20nm and W_{NW}=25nm and EOT=1.2nm) with RTN signal and without RTN signal. Noise spectrum of device without RTN is attributed to mobility fluctuation.

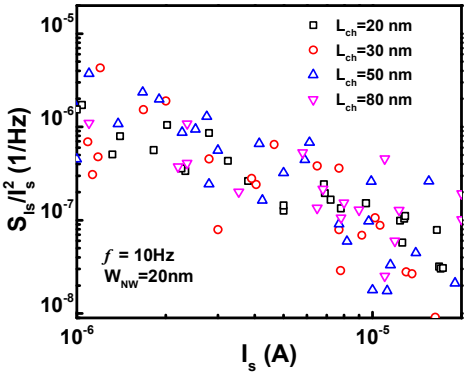

Fig. 10 Normalized I_s noise versus I_s at f=10 Hz of a InGaAs GAA nanowire MOSFET with different L_{ch}. S_{Is}/I_s^2 versus I_s shows weak L_{ch} dependence. At least 5 measured devices are shown for each L_{ch}.

at same L_{ch} [1]. Fig. 6(c) and (d) are the comparison between model and experiment which matches with each other. Series resistance (R_{sd}) can be extracted at the same time or with various different methods [28-30]. In the InGaAs nanowire devices, $R_{sd}=R_{NW}+R_{gap}+R_{barrier}+R_c$ as shown in Fig. 7. R_{sd} can be divided into two parts. R_{NW} is proportional to $1/W_{NW}$, the other is non-related part $R_{gap}+R_{barrier}+R_c$ with a constant value. By linear fitting, the non-related part can be extracted which reflects the resistance of contact and S/D sheet resistance.

B. RTN and Noise based Defect Characterization

Apart from extraction method based on I-V characteristics, low frequency noise and RTN become important probes in the characterization of short channel InGaAs nanowire MOSFETs. The systematical study of noise and RTN can be found in Ref. [13]. For the measured InGaAs GAA MOSFETs, RTN is observed in one third of devices. RTN phenomenon is shown in Fig. 8, exhibiting the trapping and de-trapping phenomenon between channel and oxide defects. For devices without RTN, mobility fluctuation is identified as the source of low frequency noise. Fig. 9 shows the comparison of noise spectrum between a device with RTN signal and a device without RTN. The two devices share the same device dimension with L_{ch}=20nm, W_{NW}=25nm and 3.5 nm Al_2O_3 as gate dielectric. It is clear that noise spectrum of the device without RTN shows 1/f characteristic while the noise spectrum of the device with RTN is the superposition of 1/f noise spectrum and a Lorentzian spectrum. Normalized I_s noise versus I_s shows weak dependence on L_{ch} , as shown in Fig. 10, while in conventional number fluctuation theory, Normalized I_s noise versus I_s should be inverse proportional to L_{ch}. This experimental results suggest oxide trapping is not the source of the 1/f noise but mobility fluctuation is the source of 1/f noise. The weak L_{ch} dependence can be explained by relatively long mean free path in InGaAs, indicating near-ballistic transport. Normalized I_s noise versus I_s (device without RTN) also shows weak dependence on dielectric material and thickness [13].

C. Self-Heating Characterization

Multi-gate structures such as FinFET and GAA nanowire MOSFET have been developed to overcome short channel effect, but heat dissipation could be a challenge, especially for GAA structures where the channel is surrounded by oxides

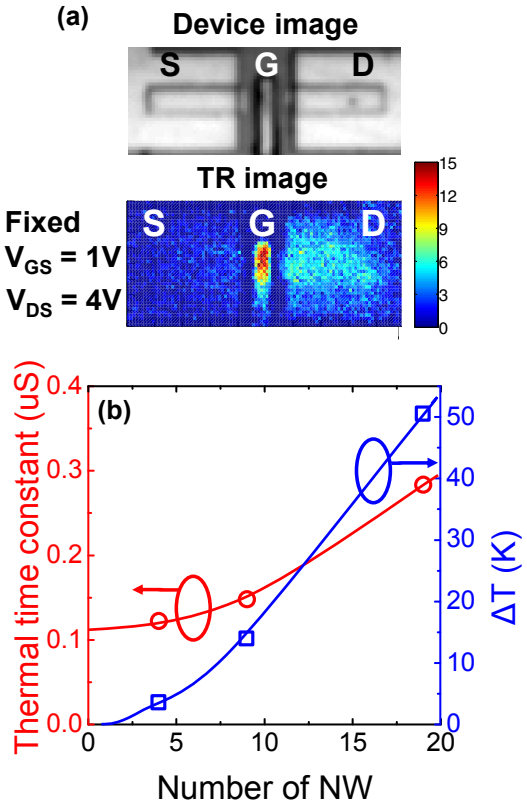

Fig. 11 (a) ΔT and power (heat) dissipation (=$V_D \times I_D$) depending at V_G=1V & V_D=4V). (b) Both ΔT (blue square) and the thermal time constants at 63% of the maximum ΔT dissipation per NW depending on the number of NWs.

and ALD-deposited gate metal, neither of which have high thermal conductivity. From these structures, therefore, the on and off-currents may degrade due to self-heating [16]. Moreover, fin-to-fin variability is an important concern, but the two electrical characterization approaches discussed in the preceding sections rely on response (current or noise) integrated over the fins.

A new optical technique, called thermoreflectance (TR) method, allows determination of self-heating and fin-to-fin variability with high accuracy [17]. This technique captures the surface temperature, ΔT (x,y,time) of the device by an ultra-fast measurement set up. Briefly, a LED pulse illuminates the device and a high speed CCD camera captures the reflected image with a time resolution of 50ns. By delaying of the LED pulse to capture a specific moment, any change in the reflectance of the LED light is captured by the image. Moreover, heating and cooling time constants can be measured by turning on and off drain bias through pulse generator, as has been discussed in [17]. With a 530nm LED, the surface temperature can be imaged in a sub-micron spatial resolution. Fig. 11a shows one example of TR image and it is observed that the asymmetry in self-heating near drain side under high bias can be correlated to the high energy dissipation at the drain-side of the transistor [16]. Fig. 11b shows that saturated ΔT and the time needed to reach the saturated temperature (thermal time constant, τ) both increase almost linearly with the number of NWs, as expected. Specifically, power-dissipation increases linearly with NW; the thermal cross-talk between NWs increases temperature. Also, it takes time to heat a larger thermal mass of a multi-NW transistor, hence the larger time constants.

To summarize, time-zero defect density, self-heating, and fin-to-fin variability are important concerns for GAA devices. These issues are inaccessible to classical characterization techniques, and therefore, a new class of techniques help determine the relevant quantities. In addition, the reliability of GAA transistors also have unique issues not found in classical devices. We will discuss these issues next.

III. Reliability of III-V GAA MOSFETs

A. Electrical Analysis

Reliability characteristics are important in CMOS applications. Reliability physics and performance should be carefully studied on InGaAs nanowire MOSFETs due to the new material and 3D structure. For example, InGaAs has a smaller bandgap (0.74eV in $In_{0.53}Ga_{0.47}As$) than Si, so that it may suffer from degradation issues accelerated by impact ionization [31, 32].

Reliability studies have been performed both on planar devices [18-25] and on nanowire MOSFETs [15, 16]. The PBTI and HCI measurements are done with an automated measure-stress-measure (MSM) setup at various bias conditions and room temperature. The full transfer characteristics are obtained during each measurement step. The results are summarized in Fig. 12 and 13.

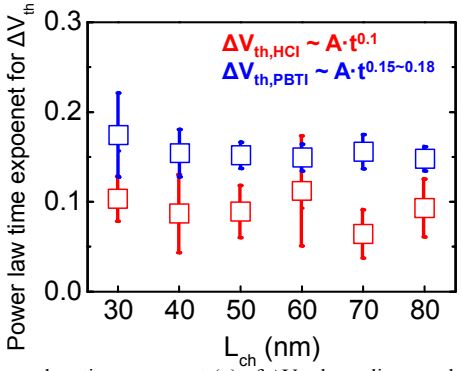

Fig. 12 Power law time exponent (n) of ΔV_{th} depending on channel length extracted from ΔV_{th} (10^1-10^4s). In a wide range of channel length, ΔV_{th} is 0.1V after 10^4s stress for both HCI and PBTI, but the time exponent (n) is 0.1 under HCI (V_G =2.0V and V_D=2.0V) (red) and the time exponent (n) is 0.15-0.18 under PBTI (V_G =1.8V) (blue) respectively.

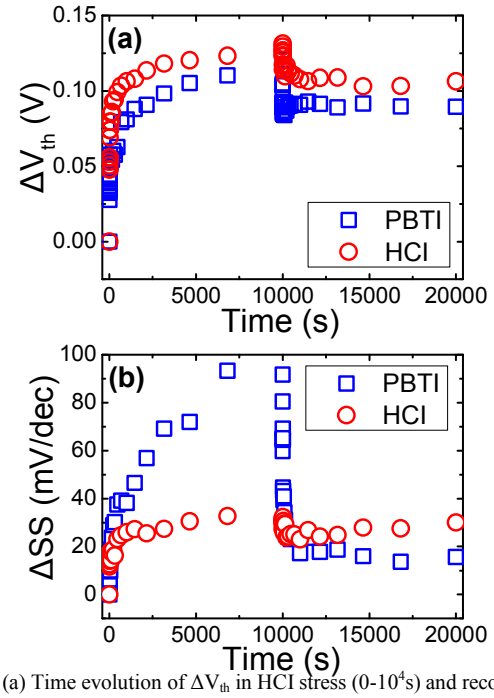

Fig. 13 (a) Time evolution of ΔV_{th} in HCI stress (0-10^4s) and recovery (10^4-2×10^4s). Initial increase in ΔV_{th} under HCI is much higher than ΔV_{th} under PBTI which is an evidence of dominant degradation mechanism is electron trapping in pre-existing trap for the HCI. (b) Time evolution of ΔSS in HCI stress (0-10^4s) and recovery (10^4-2×10^4s). ΔSS under HCI is much smaller than ΔSS under PBTI meaning that much less trap generation under HCI.

After rapid initial transient, NBTI and HCI degradation can be described by power-law degradation, namely, $\Delta V_T \sim A\cdot t^n$, where n is the time exponent [33-35]. The time-exponents associated with HCI (n_{HCI}~0.1) is considerably smaller than that of PBTI, n_{PBTI}~0.15~0.18), see Fig. 12. The stress-relaxation cycles of NBTI and HCI degradation offer further insight regarding the mechanics of these degradation mechanisms, see Fig. 13. Although ΔV_{th} are comparable for both HCI and PBTI for 10^4 sec of stress, ΔV_{th} under HCI stress shows faster initial degradation. Finally, as shown in Fig. 13b, ΔSS after 10^4 sec HCI-stress is much smaller than ΔSS after 10^4 sec PBTI-stress. Taken together, the results imply that electron trapping to the pre-existing bulk traps might be the dominant physical mechanism of the HCI degradation, while both charge trapping and newly generated

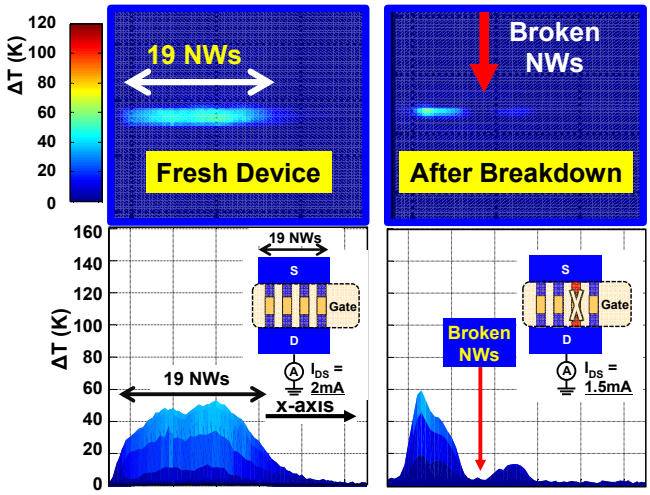

Fig. 14 TR images for 19 InGaAs NWs devices from top view at different time instant under V_G= 1 V and V_D = 2V (top) and side views are bottom. Initially, entire NWs region is bright (functioning). After stressing for certain time, one-fourth of the NWs region become dark (not functioning). Schematics of breakdown in the NWs is shown in inset and corresponding measured I_D is changed from 2mA to 1.5mA after breakdown.

interface traps are observed on PBTI degradation [16]. The trapping component will be suppressed at lower operating voltage and with improvement in oxide quality.

B. Thermoreflectance Imaging of Dielectric Breakdown

As noted previously, the electrical characterization cannot provide fin-resolved information. Therefore, the TR imaging is needed to detect variability and failure in individual NWs. Fig. 14 shows one illustrative example involving dielectric breakdown. The fresh 19NWs GAA MOSFETs had I_D=2mA. Following the TDDB stress over a prolonged period of time, one-fourth of the entire NW region becomes dark and I_D decreases from 2mA to 1.5mA; indicating that a set of NWs are broken. This observation suggests that TR-imaging can be used to study fin-resolved TDDB statistics and predict the TDDB lifetime of integrated circuits based on GAA devices.

IV. Conclusion

The methods and challenges on the characterization of 3D InGaAs MOSFETs are discussed. Reliability issues are also studied on 3D InGaAs MOSFET including PBTI, HCI and failure analysis by thermoreflectance. The GAA technology offers impressive performance; the resolution of reliability and fin-to-fin variability would ensure bright prospect for this MOSFET technology.

Acknowledgement

We acknowledge Birck Nanotechnology Center for the fabrication and characterization facilities and thanks Xiabing Lou, Xinwei Wang and Prof. Roy G. Gordon from Harvard University for the technical support in device fabrication. The work at Purdue University is supported in part by Air Force Office of Scientific Research, monitored by Dr. Kenneth Goretta and Defense Threat Reduction Agency, Basic Research Award #HDTRA1-14-1-0039.

REFERENCES

[1] J. A. del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature,* vol. 479, pp. 317-323, 2011.

[2] Y. Q. Wu, R. S. Wu, T. Shen, J. J. Gu, and P. D. Ye, "First experimental demonstration of 100 nm inversion-mode InGaAs FinFET through damage-free sidewall etching," in *International Electron Devices Meeting (IEDM) Technical Digest*, 2009, pp. 331-334.

[3] J. J. Gu, X. Wang, H. Wu, J. Shao, A. Neal, M. Manfra, R. G. Gordon, and P. D. Ye., "20-80nm Channel Length InGaAs Gate-all-around Nanowire MOSFETs with EOT= 1.2 nm and Lowest SS= 63mV/dec," in *International Electron Devices Meeting (IEDM) Technical Digest*, 2012, pp. 633-636.

[4] X. Fei, A. Jiang, Y.-T. Chen, Y. Wang, F. Zhou., Y.-F. Chang, and J. Lee., "Excellent device performance of 3D In0.53Ga0.47As gate-wrap-around field-effect-transistors with high-k gate dielectrics," in *International Electron Devices Meeting (IEDM) Technical Digest*, 2012, pp. 629-633.

[5] M. Si, J. J. Gu, X. Wang, J. Zhang, X. Li, R. G. Gordon, and P. D. Ye, "Effects of forming gas anneal on ultrathin InGaAs nanowire metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters*, pp. 093505, 2013.

[6] M., Radosavljevic, G. Dewey, D., Basu, J. Boardman, B. Chu-Kung, J.M. Fastenau, S. Kabehie, J. Kavalieros, V. Le, W.K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, L. Pan, R. Pillarisetty, W. Rachmady, U. Shah, H.W. Then, and R. Chau, "Electrostatics improvement in 3-D tri-gate over ultra-thin body planar InGaAs quantum well field effect transistors with high-K gate dielectric and scaled gate-to-drain/gate-to-source separation," in *International Electron Devices Meeting (IEDM) Technical Digest*, 2011, pp. 33.1.1 - 33.1.4.

[7] A. V. Thathachary, A. Nidhi, L. Lu, and S. Datta. "Electron Transport in Multigate $In_xGa_{1-x}As$ Nanowire FETs: From Diffusive to Ballistic Regimes at Room Temperature." *Nano letters*, vol. 14, no. 2, pp. 626-633, 2014.

[8] N. Waldron, C. Merckling, L. Teugels, P. Ong, S. A. U. Ibrahim, F. Sebaai, A. Pourghaderi, K. Barla, N. Collaert, and A. V.-Y. Thean, "InGaAs Gate-All-Around Nanowire Devices on 300mm Si Substrates." *IEEE Electron Device Letters*, vol. 35, no. 11, pp. 1097-1099, 2014.

[9] C.B. Zota, L.-E. Wemersson, and E. Lind, "In0.53Ga0.47As Multiple-Gate Field-Effect Transistors with Selectively Regrown channels," *IEEE Electron Device Letters*, vol. 35, no. 3, pp. 324-326, 2014.

[10] Y. Song, C. Zhang, R. Dowdy, K. Chabak, P. K. Mohsei, W. Choi, and X. Li, " III–V Junctionless Gate-All-Around Nanowire MOSFETs for High Linearity Low Power Applications," *IEEE Electron Device Letters*, vol. 35, no. 3, pp. 342-344, 2014.

[11] D. Jin, D. Kim, T. Kim, and J.A. del Alamo, "Quantum capacitance in scaled down III–V FETs," in *International Electron Devices Meeting (IEDM) Technical Digest*, 2009, pp. 495-498.

[12] Y. Hu, S. Li, G. Jiao, Y.Q. Wu, D. Huang, P. D. Ye and M.-F. Li, " Extraction of Channel Electron Effective Mobility in InGaAs/Al_2O_3 n-

FinFETs," *IEEE Transaction on Nanotechnology*, vol. 12, no. 5, pp. 806-809, 2013.

[13] N. J. Conrad, M. Si, S. H. Shin, J.J. Gu, J. Zhang, M. A. Alam, and P. D. Ye, "Low-Frequency Noise and RTN on Near-Ballistic III-V GAA Nanowire MOSFETs," in *International Electron Devices Meeting (IEDM) Technical Digest*, 2014, pp. 502-505.

[14] X. Sun, S. Cui, A. Alian, G. Brammertz, C. Merckling, Dennis Lin and T.P. Ma, "AC transconductance dispersion (ACGD): A method to profile oxide traps in MOSFETs without body contact.," *IEEE Electron Device Letters*, vol. 33, no. 3, pp. 438-440, 2012.

[15] S.H. Shin, M. Masuduzzaman, J.J. Gu, M.A. Wahab, N. Conrad, M. Si, P.D. Ye, and M.A. Alam, "Impact of Nanowire Variability on Peformance and Reliability of Gate-all-around III-V MOSFETs," in *International Electron Devices Meeting (IEDM) Technical Digest*, 2013, pp. 188-191.

[16] S.H. Shin, M.A. Wahab, M. Masuduzzaman, M. Si, J.J. Gu, P.D. Ye, and M.A. Alam, "Origin and Implications of Hot Carrier Degradation of Gate-all-around Nanowire III-V MOSFETs," in *IEEE International Reliability Physics Symposium (IRPS)*, 2014, pp. 4A.3.1-6.

[17] S. Shin, M. Masuduzzaman, M. Wahab, K. Maize, J. Gu, M. Si, P.D. Ye, and M.A. Alam, "Direct Observation of Self-heating in III-V Gate-all-around Nanowire MOSFETs," in *International Electron Devices Meeting (IEDM) Technical Digest*, 2014, pp. 510-513.

[18] G. Jiao, C. Yao, Y. Xuan, Da. Huang, P.D. Ye, and M.-F. Li, "Experimental Investigation of Border Trap Generation in InGaAs nMOSFETs With Al2O3 Gate Dielectric Under PBTI Stress," *IEEE Transactions on Electron Devices,* vol. 59, no. 6, pp.1661-1667, 2012.

[19] N. Wrachien, A. Cester, D. Bari, E. Zanoni, G. Meneghesso, Y. Q. Wu, P. D. Ye, "Effects of channel hot carrier stress on III–V bulk planar MOSFETs," in *IEEE International Reliability Physics Symposium (IRPS)*, 2012, pp. 3D.4.1 - 3D.4.7.

[20] N. Wrachien, A. Cester, Y. Q. Wu, P. D. Ye, E. Zanoni, and G. Meneghesso, , "Effects of positive and negative stresses on III-V MOSFETs with Al2O3 gate dielectric," *IEEE Electron Device Letters,* vol. 32, no. 4, pp. 488-491, 2011.

[21] J. Huang, N. Goel, H. Zhao, C. Kang, K. Min, G. Bersuker, et al., "InGaAs MOSFET performance and reliability improvement by simultaneous reduction of oxide and interface charge in ALD (La) AlOx/ZrO2 gate stack," in *International Electron Devices Meeting (IEDM) Technical Digest*, 2009, pp. 1-4.

[22] X. Gong, B. Liu, and Y. Yeo. "Gate Stack Reliability of MOSFETs with High Mobility Channel Materials: Bias Temperature Instability." in *IEEE Transactions on Device and Materials Reliability,* vol.13, no.4, pp.524-533, 2013.

[23] R. Wang, R. Huang, D.-W. Kim, Y. He, Wang Z., G. Jia, D. Park, Y. Wang, "New Observations on the Hot Carrier and NBTI Reliability of Silicon Nanowire Transistors," in *International Electron Devices Meeting (IEDM) Technical Digest*, 2007, pp. 821-824.

[24] J. Franco, A. Alian, B. Kaczer, D. Lin, T. Ivanov, A. Pourghaderi, K. Martens, Y. Mols, D. Zhou, N. Waldron, S. Sioncke, T. Kauerauf, N. Collaert, A. Thean, M. Heyns, and G. Groeseneken, "Suitability of high-k gate oxides for III-V devices: a PBTI study in In0.53Ga0.47As devices with Al2O3," in *IEEE International Reliability Physics Symposium (IRPS)*, 2014, pp. 6DA.2.1 – 6A.2.6.

[25] J. Franco, B. Kaczer, N. Waldron, Ph.J. Roussel, A. Alian, M. A. Pourghaderi, Z. Ji, T. Grasser, T. Kauerauf, S. Sioncke, N. Collaert, A. Thean, and G. Groeseneken, "RTN and PBTI-induced Time-Dependent Variability of Replacement Metal-Gate High-k InGaAs FinFETs," in *International Electron Devices Meeting (IEDM) Technical Digest*, 2014, pp. 506-509.

[26] Mark Lundstrom (2008), "Physics of Nanoscale MOSFETs," https://nanohub.org/resources/5306.

[27] A. Khakifirooz, O. M. Nayfeh, and D. Antoniadis. "A simple semiempirical short-channel MOSFET current–voltage model continuous across all regions of operation and employing only physical parameters." in *IEEE Transactions on Electron Devices,* vol. 56, no. 8, pp. 1674-1680, 2012.

[28] N. Conrad, S.H. Shin, J.J. Gu, M. Si, H. Wu, M. Masuduzzaman, Alam, M.A. Alam, P.D. Ye, "Performance and Variability Studies of InGaAs Gate-all-Around Nanowire MOSFETs," *IEEE Transactions on Device and Materials Reliability,* vol.13, no.4, pp.489-496, 2013.

[29] Y.-R. Kim, S.-H. Lee, C.-W. Sohn, D.-Y, Choi, H.-C. Sagong, S. Kim, E.-Y. Jeong, D.-W. Kim, H. Hong, C.-K. Baek, J.-S. Lee, and Y.-H. Jeong, "Simple S/D Series Resistance Extraction Method Optimized for Nanowire FETs," in *IEEE Electron Device Letters*, vol. 34, no. 7, pp. 828-830. 2014.

[30] J. P. Campbell, K. P. Cheung, J. S. Suehle, and A. Oates. "A simple series resistance extraction methodology for advanced CMOS devices." in *IEEE Electron Device Letters*, vol. 32, no. 8, pp. 1047-1049. 2014.

[31] M. A. Alam, J. Bude, B. Weir, P. Silverman, A. Ghetti, D. Monroe and K. P. Cheung. "An anode hole injection percolation model for oxide breakdown-the" doom's day" scenario revisited." in *International Electron Devices Meeting (IEDM) Technical Digest*, 1999, pp. 715-718.

[32] D. Varghese, V. Reddy, S. Krishnan and M. A. Alam. "OFF-state degradation and correlated gate dielectric breakdown in high voltage drain extended transistors: A review." in *Microelectronics Reliability*, vol. 54, no. 8, pp. 1477-1488. 2014.

[33] M. A. Alam, R. K. Smith, B. E. Weir and P. J. Silverman. "Thin Dielectric films: Uncorrelated breakdown of integrated circuits." in *nature*, vol. 420, no. 6914, p. 378. 2002.

[34] M. A. Alam. "A critical examination of the mechanics of dynamic NBTI for PMOSFETs." in *International Electron Devices Meeting (IEDM) Technical Digest*, 2003, pp. 345-348.

[35] H. Kufluoglu and M. A. Alam. "A geometrical unification of the theories of NBTI and HCI time-exponents and its implications for ultra-scaled planar and surround-gate MOSFETs." in *International Electron Devices Meeting (IEDM) Technical Digest*, 2004, pp. 113-116.