Anomalous Bias Temperature Instability on Accumulation-Mode Ge and III-V MOSFETs

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***Abstract*— In this work, we report the observation of anomalous bias temperature instability (ABTI) phenomenon on InGaAs accumulation-mode nMOSFET with Al_2O_3 as dielectric and Ge accumulation-mode pMOSFET with Al_2O_3/GeO_2 gate stack. During NBTI measurement on Ge accumulation-mode pMOSFETs and PBTI measurement on InGaAs accumulation-mode nMOSFETs, threshold voltage shifts to the opposite direction comparing with classic NBTI and PBTI phenomenon. A simple model is proposed to explain the experimental observation. It is understood that trap neutral level alignment and donor-like and acceptor-like traps generation and recovery are the origins of the ABTI behavior.**

***Index Terms*—Ge, InGaAs, reliability, BTI, Accumulation-mode MOSFETs.**

I. Introduction

Power consumption is one of the most critical issues in the scaling of complementary metal-oxide-semiconductor (CMOS) integrated circuits. Supply voltage reduction is required to further increase the transistor density in the future. As the decrease of supply voltage will lead to the performance degradation of the metal-oxide-semiconductor field-effect-transistors (MOSFETs), the possible use of high mobility channel materials to enhance the transistor on-state performance and to compensate the performance degradation have attracted a lot of attention and have been extensively studied. InGaAs nMOSFETs and Ge pMOSFETs are considered as strong candidates for CMOS logic in future technology for their high mobility and low carrier effective masses [1-18]. Meanwhile, people have demonstrated that using accumulation-mode devices instead of inversion-mode devices help to reduce the fermi level pinning problem in transistors with high mobility channel materials such as GaAs and Ge so that high on-current can be. People have demonstrated Ge accumulation-mode of nMOSFETs with maximum drain current exceeding 1 A/mm [15, 16], making accumulation-mode MOSFETs with high mobility channel materials promising for low power and high speed applications. However, transistors with high mobility channel materials usually suffer from high interface trap density and high border trap density compared to silicon MOSFETs. Bias temperature instability (BTI) studies on Ge and InGaAs

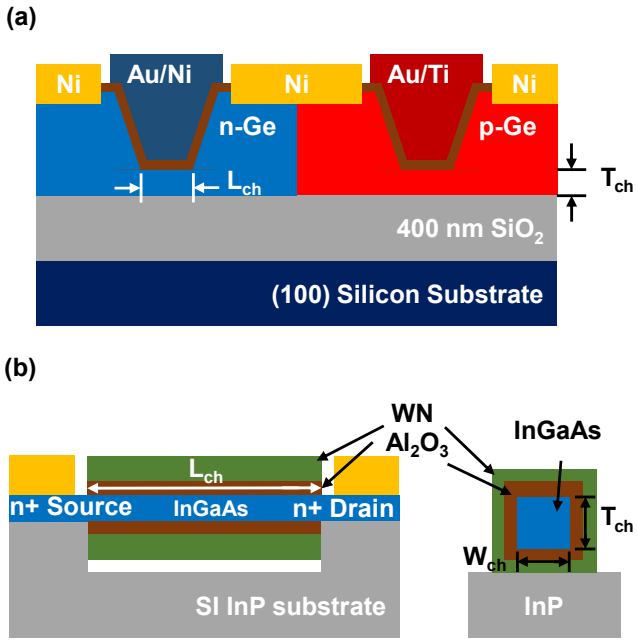

Fig. 1: (a) Schematic diagram of Ge accumulation-mode nMOSFET and pMOSFET. (b) Schematic diagram of InGaAs accumulation-mode gate-all-around nMOSFET.

have been reported showing different defects behavior [19-28]. Meanwhile, accumulation-mode MOSFETs were reported to have superior reliability over inversion-mode ones [29]. The use of accumulation-mode high mobility channel material MOSFETs may lead to high on-state performance and decent reliability at the same time. Therefore, to experimentally study and physically understand the origins of BTI on Ge and InGaAs accumulation-mode MOSFETs is important and necessary. In this work, we studied the PBTI degradation on Ge accumulation-mode nMOSFETs and InGaAs accumulation-mode nMOSFETs and NBTI degradation on Ge accumulation-mode pMOSFETs and. It is well known that if a n-type MOSFET is stressed with a positive gate bias, the threshold voltage (V_T) will shift positively because of electron charge trapping and trap generation. If a p-type MOSFET is stressed with a negative gate bias, the threshold voltage will

TABLE I. DESCRIPTIONS OF SAMPLES AND DEVICE DIMENSIONS

	Ge Accumulation-Mode pMOSFET	Ge Accumulation-Mode nMOSFET	InGaAs Accumulation-Mode nMOSFET
Channel Material	P-type Ge	N-type Ge	N-type $In_{0.65}Ga_{0.35}As$
Doping Level	Lightly doped	Lightly doped	$5\times10^{18}/cm^3$
Device Structure	Ge pMOSFET on GeOI	Ge nMOSFET on GeOI	InGaAs Gate-All-Around nMOSFET
W_{ch}/L_{ch} (μm)	1/(0.02-0.5)	1/(0.02-0.5)	1/0.4
T_{ch} (nm)	30	30	10
Gate oxide	9nm Al_2O_3/ 1nm GeO_2	9nm Al_2O_3 /1nm GeO_2	10nm Al_2O_3
EOT (nm)	4.7	4.7	4.5

shift negatively because of hole charge trapping and trap generation.

In this work, the negative bias temperature instability on Ge pMOSFETs and positive bias temperature instability on Ge nMOSFETs and InGaAs nMOSFETs are systematically studied. In spite of normal V_T shift, we observe anomalous bias temperature instability on these Ge and III-V accumulation mode MOSFETs.

- V_T shifts positively under negative stress (NBTI) and V_T shifts negatively during recovery on Ge accumulation-mode pMOSFETs (anomalous).
- V_T shifts positively under positive stress (PBTI) and V_T shifts negatively during recovery on Ge accumulation-mode nMOSFETs (normal).
- V_T shifts negatively during positive stress (PBTI) and V_T shifts positively during recovery on InGaAs accumulation-mode nMOSFETs (anomalous).

We propose a simple model to explain the experimental observation. It is understood that trap neutral level (TNL) alignment and donor-like and acceptor-like traps generation and recovery are the major origins of the anomalous BTI behavior.

II. EXPERIMENTS AND DEVICES

InGaAs accumulation-mode nMOSFETs, Ge accumulation-mode nMOSFETs and pMOSFETs are used in this work for BTI study. The device schematic for Ge nMOSFETs and Ge pMOSFETs is shown in Fig. 1(a). The Ge nMOSFETs and pMOSFETs were fabricated simultaneously on the same Ge-on-insulator substrate consisting of 180 nm (100) Ge layer, 400 nm SiO_2 buried oxide layer, and a (100) Si handle wafer. The devices featured a 30 nm channel thickness achieved through inductively coupled plasma dry etching recess, 1 nm GeO_2 and 9 nm Al_2O_3 as the gate dielectric, channel width (W_{ch}) of 1 μm and channel length (L_{ch}) from 20 nm to 500 nm. The entire contact and channel region are doped by phosphorus

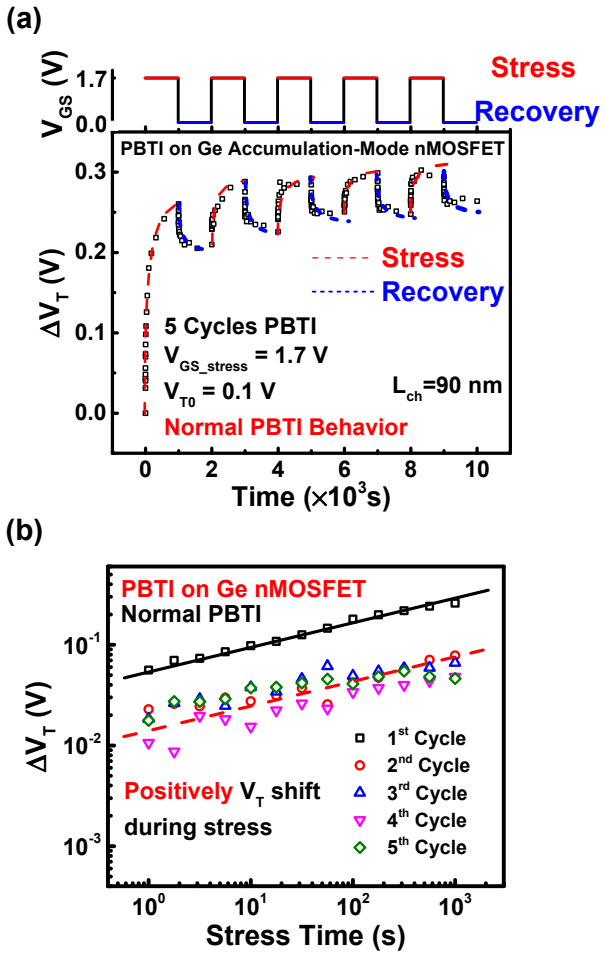

Fig. 2: (a) Time evolution of ΔV_T in PBTI on a Ge accumulation-mode nMOSFET under positive stress (V_G=1.7V) and recovery cycles (V_G=0V). PBTI on the Ge nMOSFET shows normal behavior. (b) Time evolution of ΔV_T in PBTI in different stress cycles. ΔV_T is measured by subtracting the initial V_T of each stress cycle. ΔV_T shift positively during positive stress.

implantation for n-typed Ge and BF_2 implantation for p-type Ge, so that the devices operate accumulation-mode. The InGaAs nMOSFETs were fabricated on semi-insulating InP substrates with 10 nm epitaxially grown InGaAs with 65% indium by molecular beam epitaxy (MBE), and the InGaAs channel layer was doped with $5\times10^{18}/cm^3$ silicon during the MBE growth. The devices featured a 10 nm channel thickness, 10 nm Al_2O_3 as gate dielectric, an effective channel width of ~1 μm and a channel length (L_{ch}) of 400 nm. The devices have 4 nanowires in parallel and each nanowire has a width of 100 nm, and a thickness of 10 nm. The detailed device fabrication process can be found in [2, 6].

Table 1 summarizes the descriptions of the samples and the device dimensions used for BTI characterizations in this work. The measurement was done with an automated measure-stress-measure (MSM) setup at various stress conditions. During the measurement step, a complete Id-Vg curve are measured. All threshold voltages are extracted by linear extrapolation method based on the measured Id-Vg characteristics.

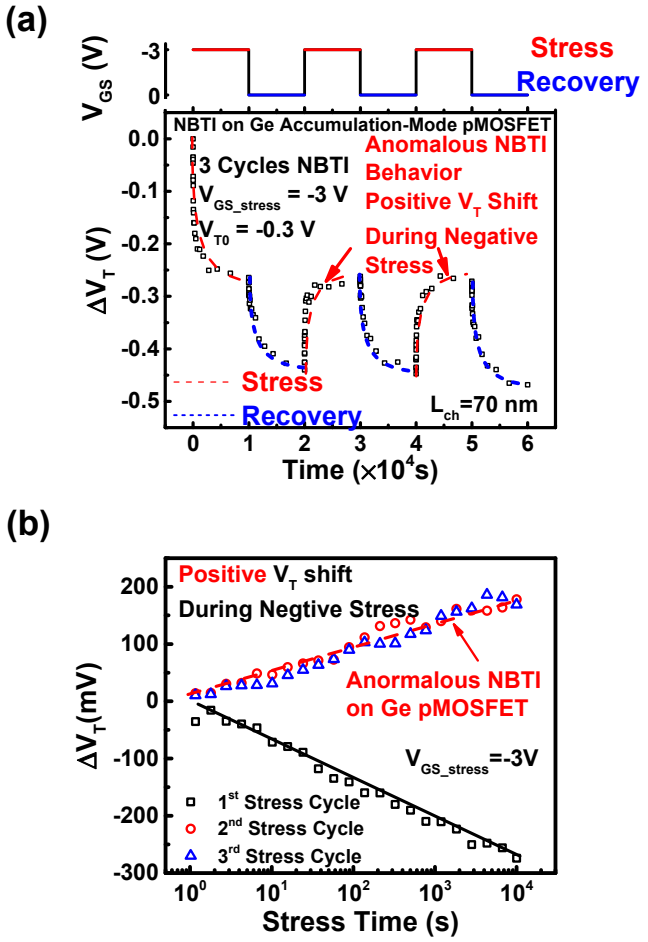

Fig. 3: (a) Time evolution of ΔV_T in NBTI on a Ge accumulation-mode pMOSFET under negative stress (V_G=-3V) and recovery cycles (V_G=0V). Anomalous NBTI appears since the 2nd cycle indicating normal NBTI only dominates the initial trapping process on pre-existing traps. (b) Time evolution of ΔV_T in NBTI in different stress cycles. ΔV_T is measured by subtracting the initial V_T of each stress cycle. ΔV_T shift positively during negative stress since the 2nd cycle which is anomalous comparing with classical NBTI measurement.

III. Obsrvation of ABTI

If a n-type MOSFET is stressed with a positive gate bias, the threshold voltage (V_T) is commonly observed to shift positively. If a p-type MOSFET is stressed with a negative gate bias, the threshold voltage is commonly observed to shift negatively. This phenomenon is widely observed on both Si and high mobility material such as III-V and Ge. And the theoretical models of NBTI and PBTI have been proposed. Normal PBTI behavior is observed on Ge nMOSFET, showing positive V_T shift during positive stress and negative V_T shift during recovery, as shown in Fig. 2(a). The devices were stressed for 5 stress and recovery cycles and each cycle lasts for 2×10^3 seconds. During stress, V_{GS} was biased at 1.7 V while V_{DS} was biased at 0 V. Fig. 2(b) shows the time evolution of ΔV_T in PBTI in different stress cycles of the same Ge nMOSFET as in Fig. 2(a). V_T shifted positively during PBTI measurement during every stress cycle. Note that during the first cycle of stress, V_T shifted much more

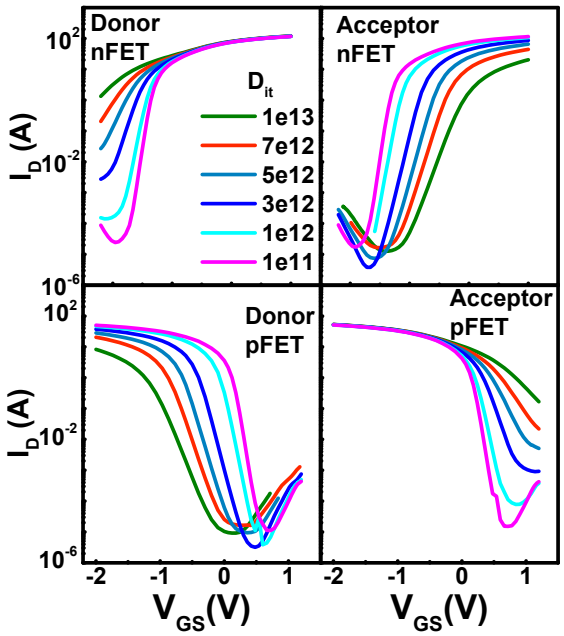

Fig. 4: (a) Simulation of nMOSFET with (a) donor-like and (b) acceptor-like interface traps and pMOSFET with (c) donor-like and (d) acceptor-like interface traps. Donor-like traps keep V_T unchanged in nFET but change V_T negatively in pFET. Acceptor-like traps keep V_T unchanged in pFET but change V_T positively in nFET.

than the other cycles because of the charge trapping in pre-existing traps and part of these traps are difficult to discharge. However, anomalous NBTI behavior was observed on Ge pMOSFET, as shown in Fig. 3(a), showing positive V_T shift during negative stress and negative V_T shift during recovery after the first cycle. The devices were stressed for 3 stress and recovery cycles and each cycle last for 2×10^4 seconds. During stress, V_{GS} was biased at -3 V while V_{DS} was biased at 0 V. As during the first cycle of stress, charge trapping in pre-existing traps dominated so that V_T shift positively as normal NBTI. As in typical NBTI measurements, V_T is observed to shift negatively during the first initial negative stress, such as NBTI in silicon pMOSFET. But it was observed that during the second and third stress cycles, V_T shifted toward the positive direction which is abnormal in NBTI measurement. Fig. 3(b) shows the time evolution of ΔV_T in NBTI of the same Ge pMOSFET. Anomalous NBTI appears from the second cycle indicating normal hole trapping in pre-existing traps process dominated the initial trapping process while ABTI dominates since the second cycle. This phenomenon is confirmed by the measurement of more than 5 chips with Ge nMOSFETs and pMOSFETs and each chip having 800 devices with L_{ch} from 20 nm to 500 nm.

IV. Understandings of ABTI on Ge and III-V MOSFETs

It is also known that mobile ions can cause the V_T shift toward the different direction comparing with charge trapping or normal generation of new traps. If the ABTI phenomenon observed here is because of mobile ions, we would observe ABTI on both Ge nMOSFETs and Ge pMOSFETs, because

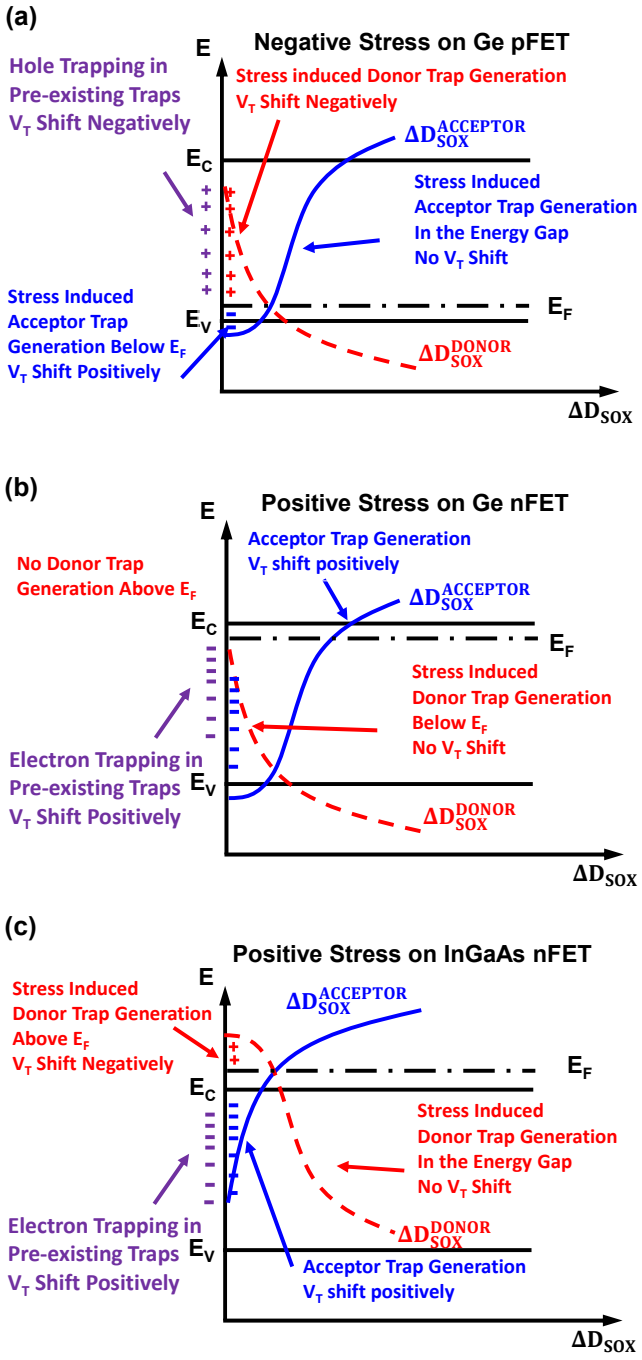

Fig. 5: Model of V_T shift of (a) negative stress on Ge pFET, (b) positive stress on Ge nFET, (c) positive stress on InGaAs nFET [21]. The alignment of trap neutral level, donor-like and acceptor-like trap generation and recovery are applied to explain the anomalous behavior.

they were processed together on the same wafer and have the same gate stack. From the observation, it is found the anomalous BTI behavior is obtained on Ge pMOSFET but not Ge nMOSFET, suggesting mobile charges are not the origin of the ABTI. As both charge trapping and mobile ions can't explain the experiments, one possible origin of the ABTI results is the generation of new traps. The difference is explained by the alignment of TNL within the energy band and donor-like and acceptor-like trap generation. It is already known that if interfaces traps are generated within the

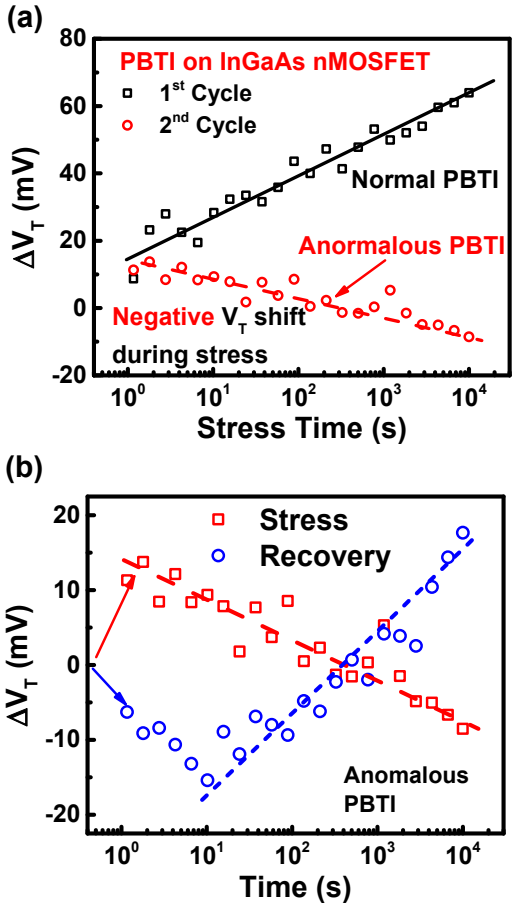

Fig. 6: (a) Time evolution of ΔV_T in PBTI of an InGaAs accumulation-mode nMOSFET. ΔV_T is measured by subtracting the initial V_T of each stress cycle. ΔV_T shift negatively during positive stress (V_{GS}=3 V) after the 1st cycle as predicted by the theory (Fig. 5(c)). (b) Time evolution of ΔV_T in the 2nd cycle of PBTI on the same InGaAs nMOSFET as shown in (a). ΔV_T is measured by subtracting the initial V_T of stress time and recovery time. Both normal PBTI and anomalous PBTI appear during stress and recovery while anomalous PBTI dominates on long time stress.

bandgap, donor-like traps keep V_T unchanged in nMOSFET but change V_T negatively in pMOSFET. Acceptor-like traps keep V_T unchanged in pMOSFET but change V_T positively in nMOSFET, as shown in Fig. 4(a)-(d) [15, 30]. Therefore, new trap generation with energy levels within the bandgap of the semiconductor can't explain the ABTI, either. We explored the possible V_T shift if new trap is generated above the conduction band (E_C) or below valence band (E_V). It is also well-known the TNL is easily aligned near the conduction band at oxide/InGaAs interface while the TNL is aligned near the valence band at oxide/Ge interface [31, 32]. Fig. 5(a) shows the model of V_T shift in NBTI on Ge pMOSFET under negative stress (V_G-V_T<0). Donor trap generation and hole trapping in the pre-existing traps will lead to a negative V_T shift. Acceptor-like traps generation above E_F does not affect V_T according to Fig. 4(d) while acceptor-like traps generation below E_F lead to a positive V_T shift because they are negatively charged. Hole trapping in pre-existing traps, donor-like traps, and acceptor-like traps generation together determine the direction of ΔV_T. In this work, acceptor-like traps generation below E_F dominates the V_T shift after the 1st

stress cycle. The acceptor-like traps generation below E_F is the only possible origin of anomalous NBTI on Ge pMOSFETs. Fig. 5(b) shows the model of V_T shift in PBTI on Ge nMOSFET during positive stress (V_G-V_T>0). In the same way, acceptor trap generation and electron trapping in pre-existing traps lead to a positive V_T shift. As TNL is aligned near the valence band, the trap states above the E_C is less likely to be a donor trap. No donor-like traps are distributed above E_F and donor-like traps generated below E_F are not charged, so V_T is not affected. Thus, no negative V_T shift happens during PBTI stress for Ge nMOSFETs. Therefore, no anomalous PBTI behavior can be observed on Ge nMOSFETs. To verify this model, PBTI is also studied on InGaAs accumulation-mode nMOSFETs. V_T shift under PBTI stress on InGaAs nMOSFETs would be different comparing with Ge nMOSFETs because of the difference in TNL position in oxide/semiconductor interface. Fig. 5(c) shows the model of V_T shift of InGaAs nMOSFET during positive stress. The difference between Ge nMOSFETs and InGaAs nMOSFETs is that the TNL of InGaAs aligns near E_C while TNL of Ge aligns near E_V. As a result, donor-like traps will distribute above E_C at the oxide/InGaAs interface but not above E_C at oxide/Ge interface. In the same way, during positive stress on InGaAs nMOSFET, acceptor trap generation and electron trapping in pre-existing traps lead to a positive V_T shift. Donor-like traps generation below E_F does not affect the V_T but Donor-like traps generation above E_F leads to a negative V_T shift. Thus, from the prediction of this model, it is possible to observe anomalous PBTI on InGaAs nMOSFETs. In the experiment, the anomalous BTI behavior is confirmed on InGaAs accumulation-mode nMOSFET. Fig. 6(a) shows the time evolution of ΔV_T in PBTI of InGaAs nMOSFET under stress of 3 V in different stress cycle. It is clearly observed in the 2nd stress cycle, V_T shift negatively. Fig. 6(b) shows the time evolution of ΔV_T in one cycle of PBTI on InGaAs nMOSFET with anomalous V_T shift. Both normal PBTI and anomalous PBTI appear during stress, indicating charging trapping and trap generation co-exist.

V. Conclusion

Anomalous bias temperature instability is observed and systematically studied on both Ge accumulation-mode pMOSFETs with Al_2O_3/GeO_2 gate stack and InGaAs accumulation-mode nMOSFETs with Al_2O_3 as the dielectric. The phenomenon can be understood by the asymmetric trap distribution model for Ge and III-V. This work motivates more comprehensive studies on reliability issues of Ge and III-V in terms of inversion-mode devices versus accumulation-mode or junction-less configuration.

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