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New insights in the passivation of high-*k*/InP through interface characterization and metal–oxide–semiconductor field effect transistor demonstration: Impact of crystal orientation

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We have systematically studied the passivation of InP (100) and (111)A substrate using atomic-layer-deposited Al_2O_3 as gate dielectric. Modified high- and low-frequency method and full conductance method has been applied to evaluate the interface trap density (D_{it}) distribution at Al_2O_3/InP interface through MOS capacitor (MOSCAP) and MOSFET measurements. Lower D_{it} towards conduction band is obtained from (111)A surface, accompanied by an increase in midgap D_{it}. This leads to the demonstration of record-high drive current ($I_{ds} = 600\,\mu A/\mu m$) for a InP (111)A NMOSFET with gate length (L_G) of 1 μm and relatively large subthreshold swing of 230 mV/dec at off-state. Detailed DC IV and current drift measurements confirm the trap distribution from capacitance-voltage characterization. A trap neutral level (E_0) model is proposed to explain all observations from MOSCAP and MOSFET characterizations. A universal behavior of the E_0 shift on III-V (111)A surface is also analyzed and this observation can play a pivotal role in interface engineering for future III-V CMOS technology with 3D structures. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4772944]

I. INTRODUCTION

III-V semiconductors have recently drawn much attention in the device community as possible alternative channel materials for future high-performance low-power logic applications.[1] In particular, the demonstration of high current drivability in inversion-mode InGaAs MOSFETs with atomic-layer-deposited (ALD) or MBE gate dielectrics[2–9] opened tremendous opportunities in further optimization of device structure and scaling of III-V MOSFETs.[10–13] InP is a widely used compound semiconductor with wide range of applications in electronics, optoelectronics, and photonic devices. Compared to GaAs, InP is widely believed to be a more forgiving material with respect to Fermi level pinning and has a high electron saturation velocity (2.5×10^7 cm/s) as well. The formation of a high quality gate dielectric on InP could therefore enable high speed transistors. It is also of great importance to understand the high-k/InP interfaces since InP has been identified as a promising barrier layer for state-of-the-art InGaAs quantum well transistors, and buried-channel InGaAs MOSFETs.[5,14]

Recently, an inversion-type enhancement-mode InP MOSFET with ALD Al_2O_3 has been demonstrated with maximum drain current of around 70 $\mu A/\mu m$ and L_G of 0.75 μm.[15] Although unpinning of the Fermi level in InP has been achieved using an ALD dielectric, the drive current of InP MOSFETs is not as impressive as that observed for InGaAs devices.[3,16] Moreover, optimization of the sulfur passivation has been shown to improve the high-*k*/InP interface and off-state performance of the buried-channel InGaAs MOSFETs.[17] This further confirms that careful surface engineering can control the quality of high-*k*/InP interface. Recently, a higher drain current has been reported on GaAs and InGaAs MOSFETs with (111)A crystal orientations.[18–20] However, a *systematic* study of high-*k*/InP MOS interface with a different crystal orientation is lacking and may illuminate on the physical origin for the improved transport property on the III-V (111)A-oriented surface. InP (111)A is In-terminated polar surface while InP (100) is a mixed In- and P-terminated polar surface.

In this paper, we study the ALD Al_2O_3/InP interface through MOS capacitor (MOSCAP) and MOSFET characterizations with a focus on the effect of crystal orientations. The InP (100) and (111)A surfaces are shown to drastically change the trap distribution in the bandgap and result in remarkably different device characteristics under various biasing conditions. A shift of E_0 is proposed as the origin for the observed differences on (100) and (111)A surfaces. The validity of this model is further confirmed by comparing results from other III-V materials such as GaAs and InGaAs. This universal D_{it} distribution dependence on crystal orientation provides unique opportunities in future interface engineering of III-V materials.

II. DEVICE FABRICATION

N-type InP (100) or (111)A substrates were used for MOSCAP fabrication. After native oxide removal using buffered oxide etch (BOE) solution and sulfur passivation (20% $(NH_4)_2S$ for 10 min), 8 nm Al_2O_3 gate dielectric were grown by ALD at 300 °C, followed by electron beam evaporation of

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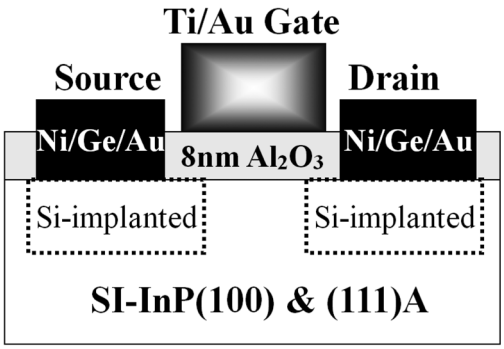

FIG. 1. Schematic cross section of the InP (100) or (111)A NMOSFETs with Al_2O_3 gate dielectric.

Ni/Au as gate electrodes. The MOSFET fabrication starts with semi-insulating InP (100) or (111)A substrates. After surface degrease, 30 nm ALD Al_2O_3 was first grown as an encapsulation layer. Source and drain regions were then selectively implanted with a Si dose of $1 \times 10^{14}\,cm^{-2}$ at 80 keV through the 30 nm Al_2O_3 layer. The dopant activation was carried out using rapid thermal annealing (RTA) at 750 °C for 15 s in N_2 ambient. The Al_2O_3 encapsulation layer was then removed by BOE. The same sulfur passivation as the MOSCAPs were then performed, followed by the regrowth of 8 nm ALD Al_2O_3 as gate oxide. Post deposition annealing using RTA at 500 °C for 30 s was then performed also in N_2 ambient. Source and drain contacts were then formed by electron beam evaporation of Au/Ge/Ni and liftoff process, followed by 400 °C RTA in N_2. Finally, the gate electrodes were patterned using electron beam evaporation of Ti/Au and liftoff. Figure 1 shows the schematic cross section of a finished ALD Al_2O_3/InP NMOSFET. The fabricated MOSFETs have a nominal gate length varying from 40 μm down to 100 nm.

III. X-RAY PHOTOELECTRON SPECTROSCOPY (XPS) CHARACTERIZATION

On both InP (100) and (111)A surfaces, the self-cleaning effect (reduction of surface oxides) by the ALD process is observed from high resolution TEM images.[21] XPS studies were carried out to further verify the interface oxide components. The samples for XPS are prepared using 2 nm Al_2O_3 with the same interface passivation as the fabricated MOSCAP and MOSFET. Figure 2 shows the In 3d and P 2p core level spectra for InP (111)A. The spectra suggest that both In^{3+} and phosphorus oxides are near or below the XPS detection limit. Compared to an XPS study on HfO_2/InP,[22] the amount of surface oxides are significantly reduced with Al_2O_3 gate dielectric.[23] Similar to the spectra reported in Ref. 22, the In^{1+} and In-S bonding is detected from the ammonium sulfide passivated samples, with the caveat of considering the potential asymmetry of the In 3d feature. Similar observations were observed on InP (100) as well. Detailed interface characterization is discussed in Secs. IV–VI through electrical measurements.

IV. CAPACITANCE-VOLTAGE (CV) CHARACTERIZATION

A. High- and low-frequency method

Temperature dependent multi-frequency CV measurements were performed on the fabricated InP (100) and (111)A NMOSCAPs, where a HP4284 LCR meter was used for the capacitance measurements. Figure 3 shows the CV response of InP NMOSCAPs at 300 K and 77 K with frequency from 1 kHz to 400 kHz. In the accumulation region, the majority carrier temperature dependent multi-frequency CV is an effective test vehicle for Fermi level pinning.[18] At 77 K, both InP (100) and (111)A do not show significant capacitance reduction in the accumulation region, indicating relatively low interface trap density in the upper bandgap for both crystal orientations, in great contrast to GaAs case.[18] However, the frequency dispersion for the InP (100) orientation is higher than that of (111)A at room temperature, indicating a higher density of traps near or inside the conduction band in InP (100). On the other hand, the large frequency dispersion in the depletion and inversion region at 300 K indicates a D_{it} in the midgap, which is greatly suppressed when temperature is cooled down to 77 K, as the minority carrier response is not sensitive at the measured frequency and a portion of the interface traps in the midgap is frozen out. The InP (111)A MOSCAP CV shows larger bumps in the inversion region at 300 K, which may indicate larger D_{it} in the midgap. To quantify the trap distribution in the midgap, we adopt a modified high- and low-frequency

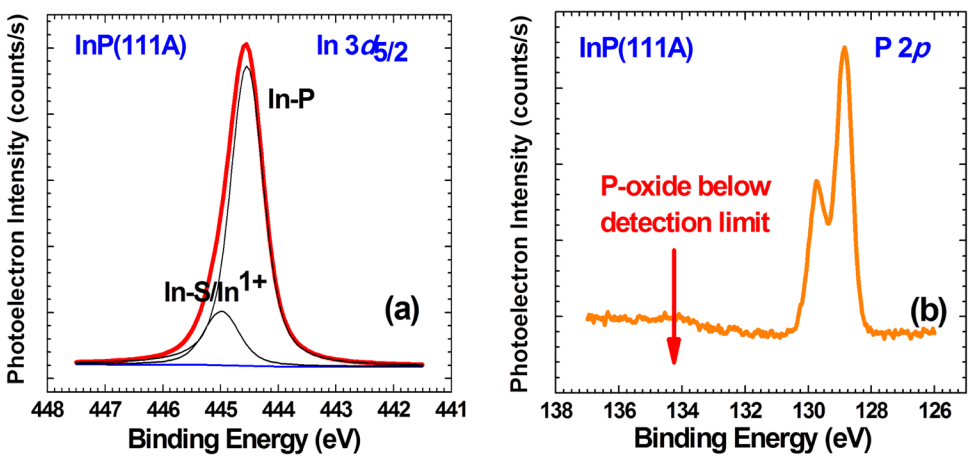

FIG. 2. High resolution XPS taken at 75° take-off angle for (a) In 3d and (b) P 2p core level spectra for 2 nm Al_2O_3 on InP (111)A.

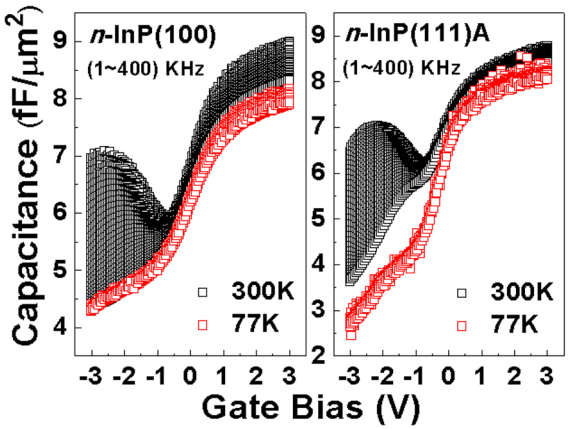

FIG. 3. CV characteristics of InP (100) and (111)A NMOSCAPs at 300 K and 77 K in frequency range of 1 kHz to 400 kHz.

method.[24] The interface trap density of a limited range in the bandgap can be determined as

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}}\right), \qquad (1)$$

where C_{ox} is the oxide capacitance, C_{lf} is the 1 kHz capacitance at 300 K, C_{hf} is the 400 kHz capacitance at 77 K, and q is the electronic charge. Figure 4 shows the D_{it} distribution in the bandgap extracted from InP (100) and (111)A NMOSCAP. The results clearly show that the InP (111)A has higher D_{it} in the bandgap than InP (100). It is noted here that the high- and low-frequency method gives D_{it} over a limited range of bandgap, from the onset of inversion towards the majority carrier conductance band (E_C) edge. Trap response near or inside the E_C cannot be extracted and require other CV techniques such as conductance method,[25] charge pumping method,[26] or MOSFET characterization.[27]

B. Full conductance method

In this section, full conductance method was applied to the MOSFET structure using temperature dependent multi-frequency CV measurements. The source and drain electrode were shorted to make a MOSFET 2-terminal device for CV measurements, similar to the configuration of a split-CV measurement. The measurement temperature was varied from 300 K up to 393 K to probe different energy regions in the bandgap. Figure 5 shows the multi-frequency MOSFET CV response at 300K and 393 K.

At 300 K, InP (111)A CV shows larger flatband voltage shift compared to InP (100). This is more significant at 393 K along with an increasing CV stretch out. These all points to a higher D_{it} near the midgap on InP (111)A, consistent with the results from high- and low-frequency method of NMOSCAP. Conductance method is applied to map the interface trap distribution quantitatively. Figure 6 shows the D_{it} distribution in the bandgap for InP (100) and (111)A from the conductance method on MOSFET structure, which agrees very well with the results from low- and high-frequency method on NMOSCAP in Figure 4. The two extractions show good agreement and the larger D_{it} near midgap of InP (111)A compared to (100) is confirmed. Note that the conductance method at the measured temperatures did not capture the majority carrier response from NMOSCAPs, where larger accumulation capacitance frequency dispersion has been observed on (100) surface. The D_{it} extraction near or inside E_C can be addressed by low-temperature conductance method, or MOSFET current-voltage (IV) measurements,[27] where the Fermi level will move inside the conduction band in the MOSFET on-state operation due to the low effective conduction band density of states in InP ($\sim 5 \times 10^{17}$ cm^{-3}).

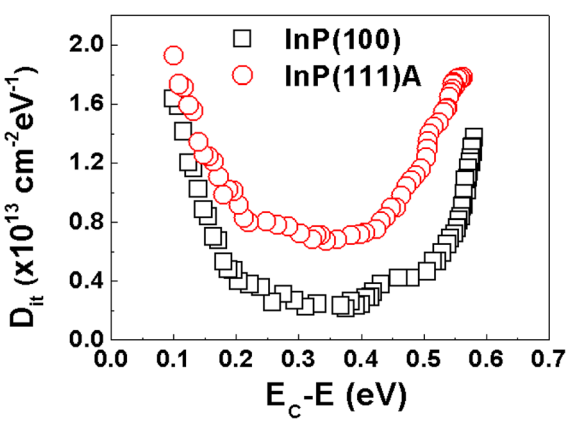

FIG. 4. Interface trap distribution in the bandgap in InP (100) and (111)A extracted from modified high- and low-frequency method on NMOSCAPs.

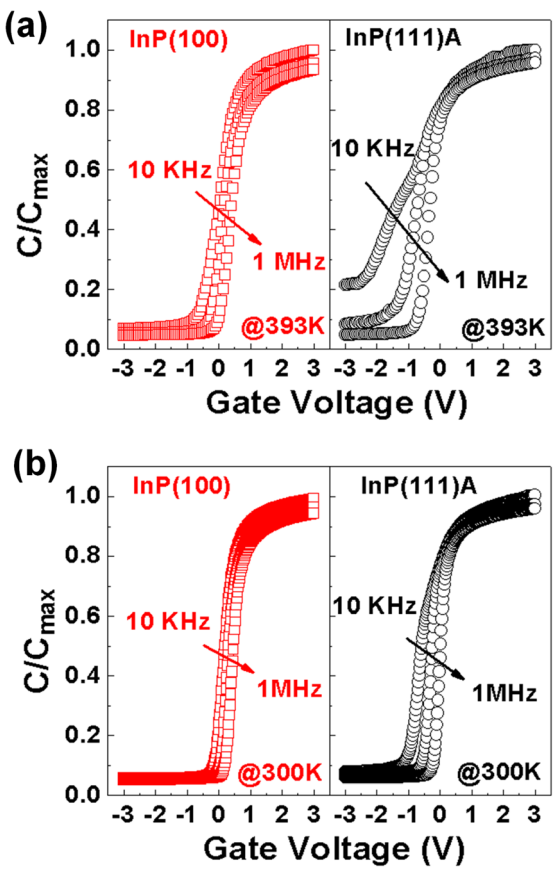

FIG. 5. Multi-frequency CV characteristics of InP (100) and (111)A MOSFET with frequency from 10 kHz to 1MHz at (a) 300 K and (b) 393 K.

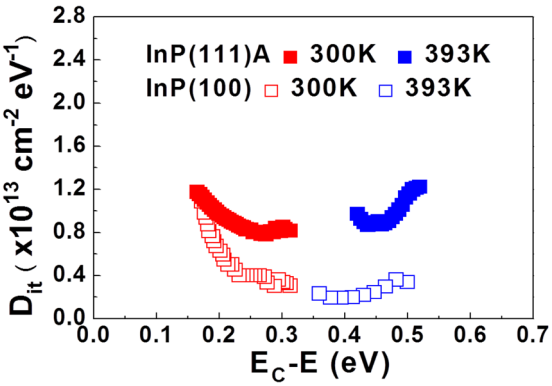

FIG. 6. Interface trap distribution in the bandgap in InP (100) and (111)A extracted from full conductance method on MOSFET compared with high- and low-frequency method on NMOSCAP.

As a summary, the CV measurements reveal that InP (111)A shows higher D_{it} near the midgap and lower D_{it} close to and inside conduction band than InP (100).

V. MOSFET CURRENT-VOLTAGE CHARACTERIZATION

A. DC IV measurements

Figure 7(a) shows the I_{ds}-V_{ds} for 1 μm L_G InP (100) and (111)A NMOSFETs. The drain current on InP (111)A is as large as 3.5 times that of InP (100) and reaches 600 μA/μm at $V_{ds} = V_{gs} = 3$V, which is, to the best of our knowledge, the highest reported drain current on inversion-type InP MOSFETs.[21] It is a factor of 2.5 times enhancement in terms of on-current if it is plotted as V_{gs}-V_T as shown in Figure 7(a). From the gate lengths dependent total resistance plot, the source/drain resistance (R_{SD}) is extracted to be 2Ω·mm for InP (111)A and 5Ω·mm for InP (100), which might also be related with the proposed E_0 model described below. Trap neutral level, which is analogous to charge neutrality level for a metal-semiconductor interface, on the (111)A surface is closer to E_C so that n-type contacts are easy to make. The source/drain diffusion length ΔL is found to be 0.4 μm due to the high activation temperature.[24] The extrinsic and intrinsic transconductance g_m-V_{gs} is shown in Figure 7(b). The maximum intrinsic g_m for InP (111)A reaches 245μS/μm at a V_{ds} of 2 V, which is also a factor of 3.5 larger than that obtained on InP (100). The advantage of InP (111)A in terms of on-current is

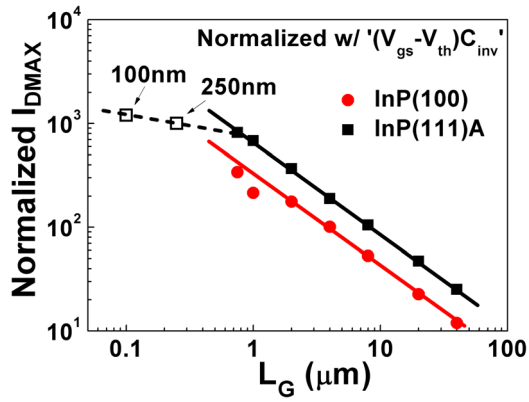

FIG. 8. Normalized maximum drain current as a function of L_G scaling for InP (100) and (111)A NMOSFETs. The measured I_{ds} is normalized with $(V_{gs}\text{-}V_{th}) \cdot C_{inv}$ for fair comparison.

demonstrated at all gate lengths, as shown in Figure 8. Good on-current scaling is obtained on both (100) and (111)A surfaces until deep-submicron L_G, where the I_{DMAX} saturates at around 1 mA/μm. Here, I_{ds} is normalized by $(V_{gs}\text{-}V_{th})\cdot C_{inv}$ for a fair comparison, where C_{inv} is extracted from split-CV measurements. The devices with L_G smaller than 300 nm can not pinch off, due to the above described ΔL and punch through in the bulk. More advanced channel doping engineering and introduction of 3-D device structures could enable the scaling of InP MOSFETs down to deep-submicron regime. The electron velocity extracted from the IV characteristics is 8.13×10^6 cm/s for InP (111)A and 2.55×10^6 cm/s for InP (100) and saturates at deep-submicron gate length with a value smaller than the thermal velocity (2.5×10^7 cm/s), due to charge transfer to the satellite valley. The effective mobility of InP (100) and (111)A MOSFETs were extracted using split-CV method as shown in Figure 9, where the inset shows the measured gate capacitance as function of gate bias at a frequency of 1MHz. The InP (111)A MOSFET shows higher effective mobility during the entire inversion charge range and reaches a peak value of $\sim$1100 cm^2/V·s at N_S of $\sim 10^{11}$/cm^2.

The on-state performance enhancement of the InP (111)A surface indicates lower D_{it} near and inside E_C, being consistent with the lower frequency dispersion in the accumulation region from NMOSCAP results. However, a clear trade-off between on- and off-state performance is observed. Figure 10 shows the transfer characteristics of a 2 μm InP (100) and (111)A NMOSFETs. The subthreshold swing (SS)

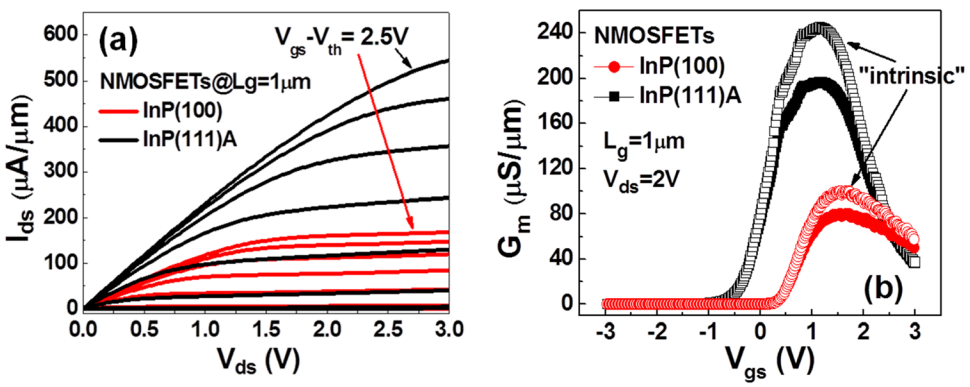

FIG. 7. (a) I_{ds} versus V_{ds} output characteristics and (b) g_m versus V_{gs} for InP (100) and (111)A NMOSFET with L_G of 1 μm.

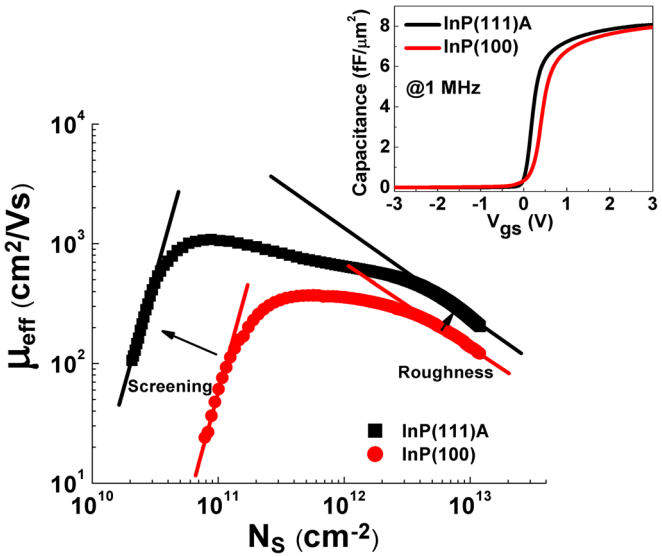

FIG. 9. Effective electron mobility versus channel inversion charge density for InP (100) and (111)A NMOSFETs. Inset: gate capacitance versus gate bias at f = 1 MHz using split-CV configuration.

for InP (111)A is 230 mV/dec, higher than 150 mV/dec from InP (100). SS is a good measure of midgap D_{it}. Ignoring the short channel effect, the SS can be expressed as

$$SS = 60\,\mathrm{mV/dec} \cdot \left(1 + \frac{C_{it}}{C_{ox}}\right), \tag{2}$$

where $C_{it} = qD_{it}$ is the interface trap capacitance and C_{ox} is the oxide capacitance. From the SS value obtained from the MOSFET IV, the upper limit of the average midgap D_{it} of InP (100) and (111)A are extracted to be 8.3×10^{12} and $1.6 \times 10^{13}\,\mathrm{cm^{-2}eV^{-1}}$, respectively. This agrees well with the D_{it} extraction from the capacitance and conductance measurements. Furthermore, the threshold voltage of the InP (111)A is 0.03 V, which is around 0.5 V lower than that of InP (100). The negative V_T shift is attributed to the lower acceptor trap density near or inside the conduction band on InP (111)A.[28] The higher midgap D_{it} is therefore mainly attributed to donor-type traps. A distribution of dominant donor-type traps and minimized acceptor-type traps pushes trap neutral level E_0 to E_C. A E_0 model will be proposed in Sec. V B to explain the differences of trap distribution on InP (100) and (111)A.

B. Drain current drift measurement

The slow drain current drift behavior peculiar to inversion-mode InP NMOSFETs is typically observed due to electron trapping near the InP/oxide interface.[29] Therefore, it is another powerful testing vehicle for probing the interface quality of high-*k*/InP. Here, the slow current drift of InP (100) and (111)A MOSFETs are systematically studied and compared. The current drift is measured by sampling the drain current I_{ds} over time after stepping the gate voltage V_{gs}. Figure 11 shows an example of the measured drain current drift of InP (100) and (111)A MOSFETs at room temperature with a V_{gs} of 3 V in linear regime. The stress time is 1200 s and the currents are normalized to the initial current $I_{ds}(t = 0)$. A striking difference between zero current drift on InP (111)A and over 10% current drift on InP (100) surface is clearly observed, similar to the saturation region.[21,30] Since the InP (111)A MOSFETs show larger output current, more inversion charge could be involved in the electron trapping and thus it is expected that InP (111)A should show worse drain current drift behavior. However, the drastically improved on-state current drift indicates that the Al_2O_3/InP (111)A is much more robust than that of Al_2O_3/InP (100) inside the conduction band. This is likely due to the reduction of acceptor traps inside the conduction band on InP (111)A surface, which in turn lowers the possibility of electron trapping in the oxide from tunneling. Similar current drift behavior is also observed at V_{gs} of 2 V. The temperature dependent drift measurements were also performed and reported elsewhere.[21]

Table I lists the drain current drift ($\Delta I_d/I_d(t = 0)$) at various biasing conditions for InP (100) and (111)A MOSFETs. The final current is sampled at t = 1200 s. In strong inversion case (on-state), the InP (100) MOSFETs show current drift in both linear and saturation regimes. Higher V_{gs} results in larger current drift, mainly due to larger band bending and more inversion charges. On the contrary, InP (111)A shows "zero" current drift at both low and high V_{ds} regardless of the $V_{gs} = 2$V or $V_{gs} = 3$V at on-state. The immunity

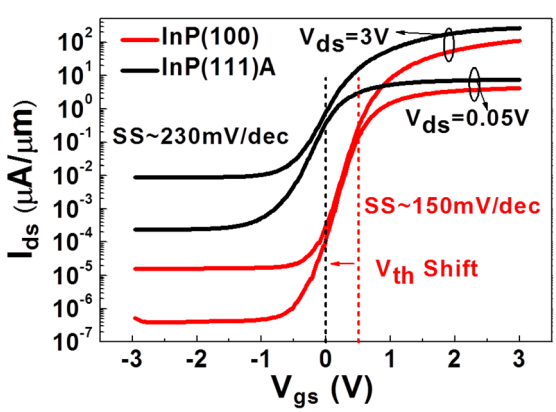

FIG. 10. I_{ds}-V_{gs} transfer characteristics of InP (100) and InP (111)A NMOSFETs with $L_G = 2\,\mu$m.

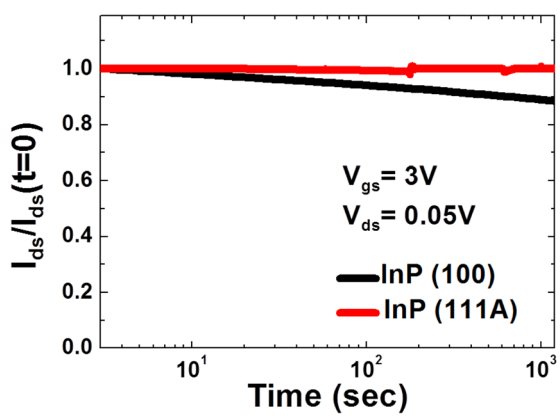

FIG. 11. Drain current drift of InP (100) and (111)A MOSFETs at 300 K with $V_{gs} = 3$V and $V_{ds} = 0.05$V. Stress time is 1200 s. Currents are normalized to the initial current $I_{ds}(t = 0)$.

TABLE I. Summary of drain current drift at different biasing conditions for InP (100) and (111)A MOSFETs.

	On-state				Off-state	
	$V_{gs} = 2V$		$V_{gs} = 3V$		$V_{gs} = -1V$	
$\Delta I_d/I_d(t=0)$	(111)A	(100)	(111)A	(100)	(111)A	(100)
$V_{ds} = 0.05V$	0%	3.5%	0%	13%	50%	0%
$V_{ds} = 3V$	0%	2.5%	0%	8%	50%	…

to current drift on InP (111)A ensures the high performance InP MOSFET with good reliability. In the off-state, however, the current of InP (100) is unchanged under stress while the InP (111)A MOSFET experiences a significant current drop. This indicates that the Al_2O_3/InP (100) interface is more stable in off-state condition where the Fermi level is located near the midgap, possibly due to a lower donor trap density than InP (111)A. In this respect, the results from current drift measurements are also consistent with our conclusion from CV and IV measurements.

VI. MODEL OF TRAP DISTRIBUTION IN III-V (111)A

In this section, all the experimental results on InP (100) and (111)A are explained by a proposed empirical trap neutral level model as shown in Figure 12. The model is also found to be universal for other III-V materials such as GaAs and InGaAs. It is strongly correlated with the unified disorder induced gap state (DIGS) model proposed in 1986 by Hasegawa and Ohno[31] and defective high-*k*/III-V interface model proposed by Robertson[32] very recently. The key point is that the interface trap distribution can be characterized by an equivalent D_{it} distribution with an energy level called trap neutral level (E_0).[33] Traps above E_0 are of acceptor type (neutral when empty, negatively charged when full), while traps below E_0 are of donor type (neutral when full, positively charged when empty). The D_{it} distribution can simply be assumed to be of parabolic shape in logarithm scale with a minimum at E_0. The minimum D_{it} and the curvature of the distribution depend on various passivation techniques. However, the location of E_0 depends on which semiconductor material and the band alignment themselves.[34,35] The solid red line in Figure 12 depicts the E_0 for InP, GaAs, and InGaAs (100) crystal orientation. This readily explains why high performance InGaAs MOSFET can be realized and achieving a large drive current remains a challenge on GaAs (100), due to the energy difference between conduction band minimum (E_C) and E_0.

Furthermore, based on the crystal orientation dependent experimental results, we propose that the E_0 shifts towards E_C on III-V (111)A surface, compared to (100).

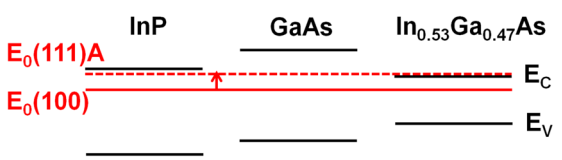

FIG. 12. Unified empirical trap neutral level (E_0) model for InP, GaAs, InGaAs (100), and (111)A. A E_0 shift towards the conduction band on (111)A crystal orientation is proposed to explain all experimental observations.

As shown in Figure 12, the E_0 on InP (111)A shifts closer to E_C. The physical origin of the E_0 shift in InP is likely related to the reconstruction of InP (111)A surface under In-rich condition.[36] In-rich surface is characterized by an In vacancy per unit (2×2) cell and found to be semiconducting, whereas the P-rich reconstruction does not obey the electron counting rule and require hydrogen passivation.[37] Although the location of $E_0(111)$A is qualitative, the model leads to the following conlusion which well explains the experimental observations on InP:

(1) Due to E_0 being closer to E_C, the donor traps below E_0 in the bandgap for InP (111)A are much higher than that of InP (100). This explains the larger trap response on InP (111)A CV measurements at depletion region; the higher D_{it} extracted from high- and low-frequency method and conductance method in the bandgap for InP (111)A; the larger SS obtained on InP (111)A NMOSFET; as well as the worse current drift behavior at off-state operation.
(2) Similarly, the acceptor traps above E_0 near or inside the conduction band for InP (111)A are much lower than that of InP (100). This explains the smaller accumulation region frequency dispersion on InP (111)A CV measurements; the higher drive current, transconductance, and effective mobility from InP (111)A NMOSFETs; the negative V_T shift on InP (111)A substrate; and the superior current drift behavior on InP (111)A in on-state operation.

The E_0 shift model is also consistent with the experimental results on GaAs and InGaAs substrates. In the GaAs case, E_0 (100) located near the midgap has impinged the efforts to realize high drive current. Significant improvements in GaAs (111)A MOSFETs, however, has been demonstrated with 5 orders of magnitude higher drive current than its GaAs (100) counterpart.[18,38] This is also well explained by the shift of E_0 closer to the E_C due to Ga-rich (111)A surface that results in much less acceptor traps preventing strong inversion on GaAs. For the case of InGaAs, similar model would lead to the $E_0(111)$A being very close to or even inside the conduction band, as also shown in Figure 12. This is again consistent with recent experimental demonstration of higher drive current and enhanced electron mobility on InGaAs (111)A,[19,39] where similar crystal orientation dependent change in trap distribution on InGaAs has been observed. All the experimental results based on various III-V (111)A substrates are accurately captured by this simple E_0 model proposed and this may serve as an important guideline for future interface engineering of high-*k*/III-V system. Note that the fundamental reason for this crystal orientation dependent D_{it} distribution could be related with the different atomic structures on different crystal oriented surfaces and their chemical bonds to the high-*k* dielectrics.

VII. CONCLUSION

In this paper, we systematically studied the CV and IV characteristics of InP MOSCAPs and NMOSFETs experimentally. High- and low-frequency method as well as

temperature-dependent conductance method has been applied to extract the D_{it} distribution inside the bandgap quantitatively. Record-high drive current has been demonstrated on InP (111)A NMOSFETs, which shows 3.5 times enhancement compared to InP (100) NMOSFETs. Negligible drain current drift is also achieved on InP (111)A NMOSFETs at on-state. To explain all the experimental results, a model of trap neutral level shift at high-*k*/InP (111)A interface is proposed and verified. Further comparison of observations on GaAs and InGaAs substrates confirms the universality of the proposed model. The observed crystal orientation dependent trap redistribution is believed to allow flexible and controllable engineering of high-*k*/III-V interfaces, which may open new opportunities in optimizing the device performance of future III-V high-speed low-power logic applications through novel 3D structure design.[10,13]

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