Minority-carrier characteristics of InGaAs metal-oxide-semiconductor structures using atomic-layer-deposited Al_2O_3 gate dielectric

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Atomic layer deposition (ALD) provides a unique opportunity to integrate high-quality gate dielectrics on III-V compound semiconductors. ALD Al_2O_3 is a high-quality gate dielectric on III-V compound semiconductor with low interface trap density, low gate leakage, and high thermal stability. The authors study the minority-carrier response of Al_2O_3/InGaAs metal-oxide-semiconductor (MOS) structures, which sheds light on the device physics for realizing high-performance inversion-type metal-oxide-semiconductor field-effect-transistor. The minority carriers in InGaAs do not respond to a small ac signal down to 100 Hz at 300 K, while they respond to up to 100 kHz at 500 K. Temperature dependent capacitance-voltage (*C-V*) measurement on the InGaAs MOS structure reveals the activation energy (E_a) of the minority-carrier recombination to be about 0.62 eV. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2357566]

Innovative channel materials, device structures, and gate dielectrics are needed to further drive Si complementary metal-oxide-semiconductor (CMOS) integration, functional density, speed, and power dissipation, and extend CMOS front-end fabrication to and beyond the 22 nm node. One emerging strategy is to use III-V compound semiconductors as conduction channels, to replace traditional Si or strained Si, while integrating these high mobility materials with high-*k* dielectrics and heterogeneously integrating them on Si or silicon on insulator. Unpinning the III-V surface Fermi level with low interface trap density (D_{it}) is the key to the realization of high-performance III-V metal-oxide-semiconductor field-effect-transistors (MOSFETs) with commercial values. For more than four decades, the research community has been searching for high-quality, thermodynamically stable insulators on GaAs that can match the device criteria as SiO_2 on Si, e.g., a mid-band-gap D_{it} of $\sim 10^{10}/cm^2$ eV.[1–8] Atomic-layer-deposited (ALD) high-*k* dielectrics on III-V are of particular interest,[9] since the Si industry is already familiar with ALD Hf-based dielectrics for front-end processes. The transition from ALD high-*k* on Si to high-*k* on III-V compound semiconductors must be easier.

In our previous work, we have succeeded in integrating ALD high-*k* dielectric Al_2O_3 on GaAs, InGaAs, and GaN, and demonstrated high-performance depletion-mode III-V MOSFETs.[9–12] But the fabricated enhancement-mode (E-mode) GaAs MOSFETs, which are of particular interest for very large scale integrated circuits or high-speed digital applications,[13,14] suffer from low drain current.[15] The minority-carrier response study could shed light on the understanding of device physics and improve the device performance. In this letter, we report detailed minority-carrier response studies on Al_2O_3/InGaAs MOS structures. The temperature dependent *C-V* measurements and revealed activation energy (E_a) of minority carrier in strained pseudomorphic InGaAs on GaAs are presented. ALD Al_2O_3 is used here as a gate dielectric. Al_2O_3 is a widely used insulating material for gate dielectric, tunneling barrier, and protection coating due to its excellent dielectric properties, strong adhesion to dissimilar materials, and its thermal and chemical stability. Al_2O_3 has a high band gap (~9 eV), a high breakdown electric field (5–30 MV/cm), a high permittivity (8.6–10), a high thermal stability (up to at least 1000 °C), and remains amorphous under typical processing conditions for implanted dopant activation on GaAs (750–850 °C). Being thermodynamically stable is very important for the gate dielectric for inversion type of E-mode III-V MOSFETs since high temperature activation of dopants is a must.

The inset of Fig. 1 shows an Al_2O_3/InGaAs MOS capacitor, which was fabricated with E-mode MOSFETs at the same time.[15] A 150 nm *p*-doped $4\times10^{17}/cm^3$ buffer layer, a 285 nm *p*-doped $1\times10^{17}/cm^3$ intermediate layer, and a 13.5 nm *p*-doped $1\times10^{17}/cm^3$ $In_{0.2}Ga_{0.8}As$ channel layer were sequentially grown by metal organic chemical vapor deposition (MOCVD) on a 2 in. GaAs p^+ substrate. After appropriate surface pretreatment, 30 nm ALD Al_2O_3 was deposited at 300 °C using an ASM Pulsar2000™ ALD module. The ALD Al_2O_3 served not only as a gate dielectric but also as an encapsulation layer due to its high thermal and chemical stability. The MOS capacitor experienced dopant activation annealing at 800 °C by rapid thermal annealing (RTA) for 10 s in N_2 ambient. The conventional Ti/Au metals were e-beam evaporated as electrodes.

The Al_2O_3 dielectric films are highly electrically insulating, showing very low leakage current density of $\sim 10^{-9}$–10^{-8} A/cm^2 at the gate bias of −15–10 V for 800 °C annealed amorphous films. Figure 1 shows typical *C-V* curves for an ALD Al_2O_3/InGaAs/GaAs MOS capacitor with an ac frequency of 100 kHz. The *C-V* measurements are widely used to quantitatively evaluate high-*k* dielectrics on novel channel materials. Three features of the *C-V* curves measured at room temperature or 300 K are of particular interest. The first is the amount of hysteresis that results

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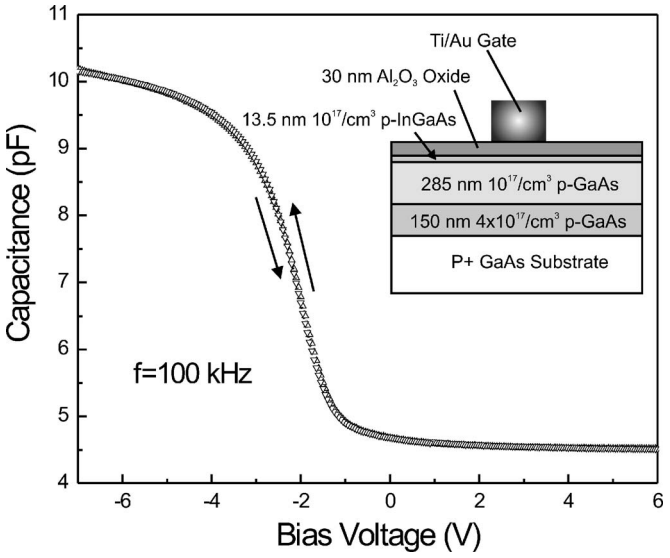

FIG. 1. *C-V* characteristics of ALD Al_2O_3/InGaAs/GaAs MOS structure at an ac frequency of 100 kHz. The up triangles are the data taken from −7 to 6 V; the down triangles are the data obtained from 6 to −7 V. The area of Ti/Au electrode is 4418 μm^2 and the MOS capacitor was measured at room temperature. Inset: Cross section of an Al_2O_3/InGaAs/GaAs capacitor fabricated for this study.

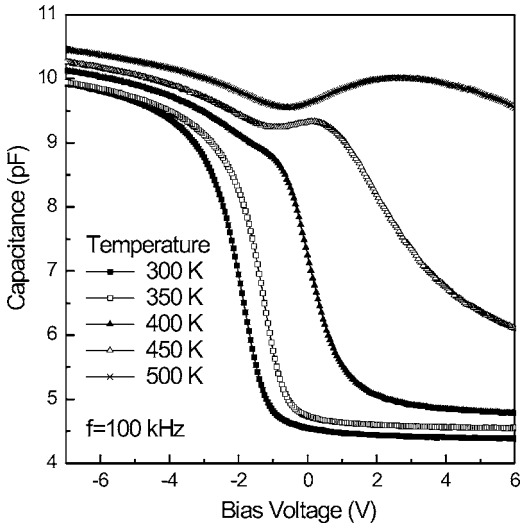

FIG. 2. Capacitance as a function of bias with temperature as parameter measured at 100 kHz. Acceptor concentration is 1×10^{17}/cm^3 and oxide thickness is 30 nm.

when the MOS capacitor is biased well into accumulation and inversion. Very small hysteresis is observed in these *C-V* sweep loops. Depending on the location of different devices and the frequency of small ac signals, the typical hysteresis is between 20 and 50 mV, corresponding to a *slow* trap density of about 5.0×10^{10}/cm^2 eV to 1.25×10^{11}/cm^2 eV. The second is the frequency dispersion on accumulation capacitances. The frequency dispersion of only 1% per decade is achieved at this frequency range.[15] The frequency dependent flatband shift is an issue for high temperature annealed films, though it is much less on medium temperature (450–600 °C) annealed capacitors and roughly scaled with the film thickness. The real origin for this frequency dependent flatband shift is unknown and still under systematic investigation. The minority carriers in InGaAs do not respond to a small ac signal down to 100 Hz at 300 K (not shown). There is no minority-carrier inversion at positive biases from 100 Hz to 1 MHz.

Temperature dependent *C-V* measurements with a wide range of small ac signal frequencies are commonly used to study the minority-carrier recombination kinetics.[16] The *C-V* measurements at 1 kHz–1 MHz and at elevated temperature from 300 to 500 K are systematically studied. Figure 2 shows the results measured at 100 kHz as a function of bias with temperature as a parameter. There is little effect on the *C-V* characteristics in accumulation and depletion over the temperature range at negative bias, though ~5% temperature dependent dispersion on accumulation capacitance does exhibit at the same level of magnitude as the frequency dispersion at accumulation capacitances.[15] The major effect of temperature occurs in inversion at positive biases. At room temperature (300 K), minority carriers do not follow the 100 kHz signal; thus a high frequency curve is measured as shown in Fig. 1. However, as temperature is increased from 300 to 500 K, minority carriers begin to follow because generation and recombination rates increase with temperature and the transition is made from a high frequency curve to a low frequency curve as shown in Fig. 2. To define a transition frequency, we regard any *C-V* curve exhibiting a minimum capacitance, such as the curve in Fig. 2 measured at 450 K, as a low frequency curve even though capacitance in strong inversion does not increase to C_{ox}. The definition is merely a matter of convenience and is arbitrary with 3%–5% error bars. Those *C-V* curves without a distinct minimum, such as the curve measured at 400 K, are considered to be of the high frequency type. The degree of recombination is limited or reduced when the bias is swept toward strong inversion or deep depletion, i.e., the 450 K *C-V* curve in Fig. 2. There is no doubt of formation of a quantum well in InGaAs between Al_2O_3 and GaAs. As the gate bias is increased or swept toward the GaAs channel, the inversion charge will be decreased due to the lower intrinsic carrier concentration of GaAs compared to that of InGaAs. Therefore, the total amount of inversion charge will be reduced, thus decreasing the capacitance in strong inversion for the 450 K *C-V* curve. The same behavior can also be observed in the 500 K *C-V* curve at the gate bias voltage larger than 3 V.

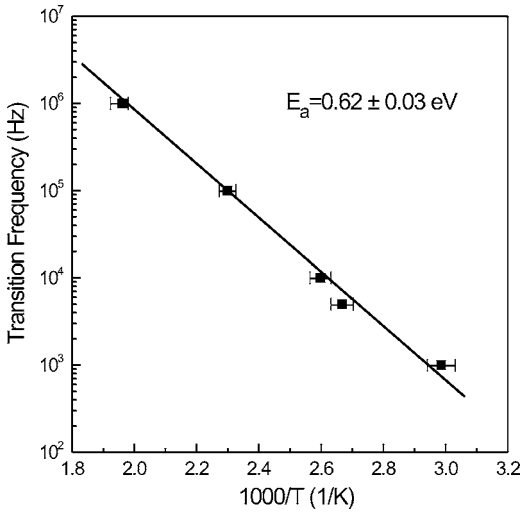

FIG. 3. Temperature dependence of the transition frequency between high and low frequency *C-V* curves. Activation energy of the minority-carrier recombination is obtained from the slope of the linear fitting trace.

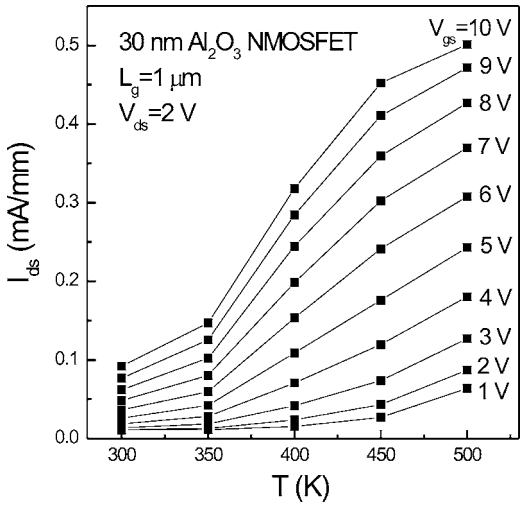

FIG. 4. Temperature dependence of the drain current at V_{ds}=2 V of a 1 μm gate length inversion channel enhancement-mode InGaAs MOSFET with a 30 nm ALD Al_2O_3 as a gate dielectric.

By systematically varying both temperatures and measurement frequencies, the temperature dependence of the transition frequency can be determined. In order to have more insights on minority-carrier response kinetics, we calculate the activation energy (E_a) of minority-carrier generation and recombination for Al_2O_3/InGaAs/GaAs MOS structures. The E_a is determined by the slope of the transition frequency versus $1/T$ plot as shown in Fig. 3. The transition frequency has an activation energy of 0.62 eV with an error bar of 0.03 eV. The measured value is very near the calculated value of 0.64 eV, the half of the band gap energy of $In_{0.2}Ga_{0.8}As$. This activation energy is that of intrinsic electrons in $In_{0.2}Ga_{0.8}As$. Therefore, the dominant mechanism for controlling minority-carrier response must be generation and recombination through bulk traps in the measured MOS structures over the temperature range of 300–500 K. The E_a is also determined to be 0.71 eV in Al_2O_3/GaAs MOS structure, which is about half of the band gap energy of GaAs. Considering similar results from MOCVD grown InGaAs and GaAs presented here, from molecular beam epitaxy grown GaAs,[16] and from *n*-type, *p*-type, and gold doped *p*-type Si,[17] the conclusion that the E_a is that of intrinsic concentration n_i or half the band gap energy is quite general.

A submicron enhancement-mode *n*-channel InGaAs MOSFET with ALD Al_2O_3 as a gate dielectric was demonstrated in the previous publication.[15] The MOSFET is fully turned on as the gate voltage varies from 0 to 12 V and the threshold voltage V_T is ~0. The realized maximum drain current on this device is only ~0.12 mA/mm so far, though it clearly demonstrates that the true inversion *n* channel can be formed at ALD Al_2O_3/InGaAs interface. The low drain current could be improved by optimizing implant and annealing conditions to reduce parasitic resistance and surface scattering. Motivated by the above *C-V* studies on minority-carrier response, we measured the *I-V* characteristics of a typical 1×100 μm^2 gate geometry MOSFET at the elevated temperatures and plot the drain current at a fixed drain bias of 2 V versus measured temperatures as a function of gate bias in Fig. 4. The elevated temperature generates more minority carriers (electrons) into the inversion channel in the E-mode MOSFET and boosts the drain current by a factor of ~5–10 depending on gate biases. At least three factors have effects on the inversion channel drain current. The intrinsic minority-carrier concentration is significantly increased by approximately six orders of magnitude from 300 to 500 K. The band gap of InGaAs or GaAs is reduced by ~10% from 300 to 500 K. Electron channel mobility is reduced at elevated temperatures due to increased phonon scattering. The effect of bulk traps from intrinsic MOCVD grown materials or most likely induced from implantation and high temperature annealing is under systematic investigation. How to increase the minority carriers from materials and device structures could be another challenge to realize high-performance inversion channel III-V MOSFETs.

In summary, we have systematically studied minority-carrier characteristics of an ALD Al_2O_3/InGaAs/GaAs MOS structures after 800 °C RTA. The leakage current remains extremely low, while *C-V* curves show extremely small hysteresis in *C-V* loops and less than 1% per decade frequency dispersion at accumulation capacitance. The temperature dependent *C-V* measurements revealed an activation energy of 0.62 eV for the minority-carrier response of the Al_2O_3/InGaAs/GaAs MOS interface. Meanwhile the drain current of the fabricated inversion-type E-mode *n*-channel InGaAs MOSFET is able to be boosted by a factor of 5–10 at the elevated temperatures, which is consistent with the well-known physical picture of minority-carrier response kinetics.

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