# Chapter 7
# Atomic-Layer Deposited High-k/III-V Metal-Oxide-Semiconductor Devices and Correlated Empirical Model

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**Abstract** Si CMOS scaling is reaching its physical limit at the 15 nm technology node and beyond. III-V compound semiconductor is one of the leading candidates to replace main-stream Si as n-channel material due its much higher electron mobility. Lacking a suitable gate insulator, practical III-V metal-oxide-semiconductor field-effect transistors (MOSFETs) remain all but a dream for more than four decades. The physics and chemistry of III-V compound semiconductor surfaces or interfaces are problems so complex that even after enormous research efforts understanding is still limited. Most of the research is focused on surface pretreatments, oxide formation and dielectric materials. Less attention is given to the III-V substrate itself. In this chapter, the history and present status of III-V MOSFET research is briefly reviewed. An empirical model for high-k/III-V interfaces is proposed based on the experimental works we performed on III-V MOSFETs using ex-situ atomic-layer-deposited high-k dielectrics and also reported works in the literature using in-situ molecular beam expitaxy grown $Ga_2O_3(Gd_2O_3)$ as gate dielectric. The results show that physics related to III-V substrates is as important as surface chemistry and gate oxide properties for realizing high-performance III-V MOSFETs. The central concept of this empirical model is that the band alignment between trap neutral level ($E_0$) and conduction band minimum (CBM) or valence band maximum (VBM) and the magnitude of interface trap density governs the device performance of inversion-mode III-V MOSFETs.

## 7.1 Introduction

GaAs metal-oxide-semiconductor field-effect transistors (MOSFETs) have been a subject of study for more than four decades. The renewed research thrust is for advanced ultra-large-scale-integration (ULSI) digital applications or complementary

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metal-oxide-semiconductor (CMOS) technology beyond the 22-nm node by using III-V compound semiconductors as conduction channels to replace traditional Si or strained Si, integrating novel high-k dielectrics with these high mobility materials, and heterogeneously incorporating them on Si or silicon-on-insulator (SOI). The lack of high-quality, thermodynamically stable gate dielectric insulators on GaAs or III-V that can match device criteria similar to $SiO_2$ on Si, remains the main obstacle to realizing a III-V MOSFET technology with commercial value. The understanding of the interface physics and chemistry of the III-V's is still quite limited, though enormous research efforts have been invested in this field. The literature on this subject is spread over the last 40 years and appears in many journals and conference proceedings. Understanding these literatures requires considerable efforts by the seasoned researchers, and even more for those who are new in the field. The first part of this chapter provides the readers with a brief overview on history and current status of III-V MOSFET research. The second part of this chapter proposes an empirical model based on trap neutral level ($E_0$) concept at oxide/semiconductor interface to explain all experimental works on III-V MOSFETs using ex-situ atomic-layer-deposited (ALD) high-k dielectrics and also in-situ molecular beam expitaxy (MBE) grown $Ga_2O_3(Gd_2O_3)$ gate dielectric. The third part of the chapter provides more detailed experimental results on different ALD high-k dielectrics and different III-V substrates to verify the validation of the empirical mode. The investigated III-V substrates include $In_xGa_{1-x}As$ (x = 0, 0.2, 0.53, 0.65, 0.7, 0.75, 1), InP, InSb, GaN, and GaSb. The studied ALD high-k dielectrics include $Al_2O_3$, $HfO_2$, and their HfAlO nanolaminates.

## 7.2 History and Current Status

The advantage of GaAs MOSFET over its Si counterpart has long been recognized because the bulk electron mobility in GaAs (8800 $cm^2$/Vs) is five or more times higher than that in Si. The electron mobility advantage for InSb is astonishing as high as 77000 $cm^2$/Vs. The GaAs MOSFET research has its own phenomenal cycles coincidently with the well-know ten-year semiconductor industrial business cycles. The first GaAs MOSFET work was reported by Becke and White by the Radio Corporation of America in 1965 [1, 2]. Although deposited $SiO_2$ is used as the gate dielectric with large amount of interface traps, the devices are operated successfully at several-hundred-megahertz frequency range showing the feasibility of this approach. It was quickly realized that $SiO_2$ is not the right gate dielectric for GaAs, which ignited an enormous research effort in the following decades searching for a low-defect, thermo-dynamically stable gate dielectric for GaAs. The efforts could be divided into two scenarios: (a) deposited oxide, and (b) native oxide.

A variety of dielectrics and techniques have been investigated. The well studied dielectrics on GaAs include pyrolytically deposited silicon dioxide [1], silicon nitride [2], silicon oxynitride [3], and aluminum oxide [4]. All these processes require relatively high temperatures ranging from ~350 to ~600 °C. The chemical

reaction between GaAs and oxygen in the gas ambient is expected to form Ga-oxide, As-oxide, remaining elemental As and sometimes even a large amount of vacancies due to the high volatility of As. A low-temperature process is believed to be essential for obtaining a high-quality interface [5]. Plasma-enhanced deposition with the process temperature lower than 200 °C was attempted [6], though it could potentially induce more defects or fixed charges on GaAs surface or interface due to the plasma damage effects.

Except for the conventional physical vapor deposition (PVD) and chemical vapor deposition (CVD), the molecular beam epitaxy (MBE) approach was also used to form insulating films on GaAs after it started to be widely used to grow III-V compound semiconductor heterostructures at the end of 1970s. For example, highly resistive AlGaAs [7] or low-temperature grown GaAs [8] was used as insulating layer for GaAs channel. But the relatively high gate leakage current limits the wide application of these approaches. To improve the barrier heights at the heterojunction interface, thermal oxidation of AlAs epi-layers grown on GaAs using MBE was also investigated [9]. The difficulty of this approach is to control the oxidation process to terminate at the AlAs-GaAs interface, though the large difference in the rate of oxide formation of AlAs and GaAs exists. The research in this direction is still active currently [10].

Motivated by the success of thermal oxidized $SiO_2$ on Si, using native oxides on GaAs as gate dielectrics was also intensively studied at the very beginning. Some representative approaches include thermal oxidation [11], wet chemical anodization [12–13], dc and RF plasma oxidation [14–18], laser-assisted oxidation [19], vacuum ultraviolet photochemical oxidation [20] and photo-wash oxidation [21]. Any of these is not optimistic as a feasible approach leading to a commercial GaAs MOSFET technology. One general observation is that the native oxide is not stable, mostly leaky with low dielectric breakdown strength, and cannot be forward biased beyond a few volts. All these studies are essential to enrich our understanding of chemistry and physics properties of III-V interfaces. Although there are some controversies within a large amount of experimental data, a consensus emerges that a significant amount of $As_2O_3$, $As_2O_5$ and elemental As present in native oxides pin the Fermi-level of GaAs and are not favorable for an ideal gate dielectric. The book "Physics and Chemistry of III-V Compound Semiconductor Interfaces" edited by C.W. Wilmsen and published in 1985 summaries most of experimental work in 1970s and the beginning of 1980s [22]. Recent work reveals that controlling the oxidation state of Ga at the interface ($Ga_2O$ vs. $Ga_2O_3$), formed from native oxide or ALD processes, could also play a critical role on unpinning of Fermi level on GaAs [23, 24].

A variety of models on semiconductor interfaces have also been developed at the same period of time beyond the Mott-Schottky model in 1938, J. Bardeen's surface states model in 1947 and P.W. Anderson's electron affinity model in 1962. Some representative works include Cowley and Sze's interfacial layer model in 1965 [25], Heine's metal induced gap state (MIGS) model in 1965 [26], Tejedor and Flores' model on line-up at charge neutrality level (CNL) in 1978 [27], Spicer's unified defect model (UDM) in 1980 [28], Hasegawa and Ohno's disorder-induced gap state (DIGS) model in 1986 [29], and Tersoff's dielectric midgap energy model

in 1984 and 1985 [30, 31]. All these works have strong influences on semiconductor device research including III-V MOS. For examples, W.E. Spicer's extensive experiments, published in 1980, concludes that the Schottky-barrier formation on III-V semiconductors is due to defects formed near the interface by deposition of metals or any chemisorption of oxygen [32]. This model also applies to formation of states at the III-V oxide interface. Fermi-level position in GaAs is pinned at the mid-gap no matter whether it is metal-semiconductor or oxide-semiconductor interface. This UDM doesn't persist with the modern oxide deposition techniques such as MBE and ALD with selective oxides. Very recently, J. Robertson presented a generalized model of the density of interface states at III-V oxide interfaces [33]. In this chapter, Ye (one of the authors) proposes an empirical model, refined from Refs. [34–36], in the second portion of this chapter. This empirical model is supported by a large amount of experimental work done in Ye's group at Purdue and also other groups worldwide. Some of the original ideas of this model could be tracked back to Hasegawa's DIGS' model proposed two decades ago [29].

Fermi-level pinning in III-V semiconductors stymies the enthusiasm among III-V researchers to compete with Si in large-scale integrated circuit front. But significant progress was made on high-performance microwave GaAs metal-semiconductor field-effect transistors (MESFETs) pioneered by Hooper and Lehrer [37] using GaAs Schottky barrier directly. The development of MBE and metal-organic CVD technologies in the 1970s made heterojunctions, quantum-wells, and superlattices practical. At Bell Labs, Dingle et al. first demonstrated the enhancement of mobility in the AlGaAs/GaAs modulation-doped superlattice in 1978 [38]. Stormer et al. subsequently reported similar effect using a single AlGaAs/GaAs heterojunction [39] which leads to the discovery of fractional quantum Hall effect in 1981. In 1980, Mimura et al. applied a similar concept and invented high electron mobility transistors (HEMT) [40]. Similar work was also reported later in the same year by Delagebeaudeuf et al [41]. GaAs HEMT eventually becomes a commercialized technology and finds its wide applications in communication, military and aerospace industry today. GaAs MOSFET research was not continued at a large scale after the successful introduction of GaAs HEMT.

The research work on search for suitable dielectrics or passivation layers on GaAs continues. In 1987, researchers at Bell Labs discovered that a class of sulfides [$Li_2S$, $(NH_4)_2S$, $Na_2S{\cdot}9H_2O$, etc.] are able to passivate GaAs surface and provide excellent electronic properties to GaAs surfaces [42, 43]. The work generated new interests in GaAs MOSFETs using sulfur passivation before dielectric deposition. Hundreds of papers were published related with GaAs sulfur passivation. But sulfur passivation didn't become a widespread technology since sulfur is not a stable material with very low thermal budget. Nevertheless, it is still very interesting scientifically. Sulfur, as a VI element next to oxygen, has the same electron number in its outer shell as oxygen, but less chemically reactive. It could passivate pristine GaAs surface with a few monolayers of sulfur in certain conditions and prevent GaAs from oxidation to form As-oxides. Sulfur passivation is still used in today's research. However, sulfur layers could serve as protective layers for III-V surface oxidization in ALD process. Other works on effective passivation of GaAs using

hydrogen or nitrogen plasma were also reported by IBM group [44]. Another interesting approach is to use a very thin amorphous or crystalline Si layer as an interfacial control layer (ICL) between GaAs and $SiO_2$ or $Si_3N_4$ [45–48]. This approach has been intensively studied in 90s [49–51] and recently also adopted to integrate with high-k $HfO_2$ gate dielectrics on GaAs [52–55]. Promising results are obtained on GaAs MOSFETs using $SiH_4$ passivation [56, 57], which is believed to form 1 to 2 nm interficial $SiO_2$ layer also except oxide reduction by hydrogen environment. The details of this work are reviewed in Chaps. 8 and 11 in this book.

In 1995, M. Passlack and M. Hong at Bell Labs reported that in-situ deposition of $Ga_2O_3(Gd_2O_3)$ dielectric film on GaAs surface by electron beam evaporation from single-crystal $Ga_5Gd_3O_{12}$ produced MOS structures on GaAs with a low $D_{it}$ [58–60]. Since the experiment is realized in an ultra-high-vacuum (UHV) multi-chamber MBE system, it is referred to as MBE grown $Ga_2O_3(Gd_2O_3)$ most of the time. A series of device work, mainly led by M. Hong and F. Ren, were carried out at Bell Labs after this breakthrough in material science. It includes GaAs depletion-mode (D-mode) and enhancement (E-mode) MOSFETs [61, 62], InGaAs enhancement-mode MOSFETs [63], GaAs complementary MOSFETs [64] and GaAs power MOSFETs [65]. This $Ga_2O_3(Gd_2O_3)$ dielectric device work continues at Agere Systems [66], a spin-off from Bell Labs and Lucent Technologies, and National Tsinghua University (NTHU) in Taiwan. Inversion-mode InGaAs NMOSFETs with outstanding on-state performance are reported by Hong's group at NTHU in 2008 [67]. In 2003, Passlack et al. at Motorola/Freescale started to report a series of works by modifying the previous $Ga_2O_3(Gd_2O_3)$ dielectric process and using $Ga_2O_3$ template in $Gd_xGa_{0.4-x}O_{0.6}$/$Ga_2O_3$ dielectric stacks on GaAs [68]. An implant-free enhancement-mode device concept was introduced and good device performance was demonstrated in 2006 to eliminate the difficulty to realize the inversion-operation due to the relative low thermal budget of III-V and gate dielectric stacks [69]. The work continues as a collaborative effort at the University of Glasgow [70]. UHV scanning tunneling microscopy study reveals that the unpinning of GaAs Fermi level results from $Ga_2O$ restoring the surface arsenic and gallium atoms to near-bulk charge [71].

ALD is an ex-situ, robust, and manufacturable process, which attracts wider interests in academia and industry. At the end of 2001, Ye and Wilk at Bell Labs/Agere Systems, started to work on ALD high-k $Al_2O_3$ and $HfO_2$ on GaAs and other III-V materials. A series of D-mode MOSFETs on GaAs, InGaAs and GaN using ALD $Al_2O_3$ as gate dielectrics were demonstrated [72–76]. The work on ALD integration with high-mobility channel materials continues and enhances in Ye's group at Purdue University. Detailed interface studies were carried out to demonstrate the unpinning of Fermi-level in InGaAs and GaAs (111)A surface [24, 35, 77–82] including the fundamental understanding of ALD chemical process on GaAs reported by other groups [83–86]. The "self-cleaning" effect on III-V by ALD is believed important to clean up As-oxide and provide high-quality high-k/III-V interfaces. High-performance inversion-mode III-V MOSFETs were demonstrated with unprecedented drain current as high as 1.1 A/mm and transconductance as high as 1.3 S/mm [87–93]. This is the first surface channel device in III-V with drain current beyond 500 mA/mm by reporting time and

with transconductance beyond 1 S/mm among any reported III-V MOSFETs with oxide as a gate dielectric. Even further, InGaAs FinFETs with 40 nm fin width and 100 nm gate-length are demonstrated experimentally using ALD $Al_2O_3$ [94]. In-rich InGaAs is identified as the potential channel material for future 15 nm technology node or beyond with higher effective mobility and manageable bandgap for low drain voltage. The fundamental understanding on this successful demonstration is explained by the proposed empirical model. Device process and results are briefly described in the third portion of this chapter. Currently, many research groups including Intel, IBM, IMEC, SEMATECH, UCSB III-V CMOS Center, Stanford, MIT, UT Austin, UT Dallas, NTHU, and many others are working on inversion-mode ALD high-k/InGaAs MOSFETs [95–100]. Many of the results are reviewed elsewhere in this book.

The new cycle of interest in III-V MOSFETs was initiated by Intel in 2005 for alternative device technologies beyond Si CMOS. III-V is one of its main focuses with the excellent publications on InSb-based quantum well transistors in collaborations with QinetiQ [101–102]. P-channel InSb quantum well transistors, another hassle in III-V field due to low hole mobility, with outstanding performance was also reported in IEDM 2008 [103]. Some fine experiments based on In-rich InGaAs and InAs heterostructures were also carried out at MIT J. del Alamo's group to investigate the ultimate transport properties of III-V for logic applications [104, 105]. We are hoping that the current III-V research in Si CMOS community is at the similar stage as high-k concept was introduced at the end of 1990s. After collective efforts in academia and industry, we are able to make this long-standing GaAs MOSFET dream become a real commercial technology as the successful story of high-k in Si CMOS.

## 7.3 Empirical Model for III-V MOS Interfaces

ALD is based on the self-limiting chemical reactions to form ultra-thin, uniform, conformal, and pin-hole free films. The ALD or Atomic-layer epitaxy (ALE) concept was invented in 1970s. Strong interest in non-native oxides for Si CMOSFETs began in the mid-1990s. High-k dielectric research, especially the development of ALD high-k dielectrics for Si MOSFETs, has since flourished [106]. In 2007, Intel claimed its successful integration of ALD Hf-based high-k dielectric and metal gate process into its 45 nm node technology as one of the biggest technical leaps in Si CMOS development, after the introduction of poly-silicon gate in the 1960s. The success of ALD high-k dielectrics on Si has created much more research on ALD itself and other applications beyond Si CMOS.

ALD shows its uniqueness in high-k/III-V integration. First, the ALD dielectric process, in particular, trimethylaluminum (TMA)-related $Al_2O_3$, enables unpinning the Fermi levels on most of III-V semiconductors so far studied. $Al_2O_3$ is a highly desirable gate insulator from both physical and electrical standpoints. $Al_2O_3$ has a wide bandgap (~9 eV), high breakdown field (~10 MV/cm), high thermal stability

(>1000 ºC), and remains amorphous under typical IC processing conditions. $Al_2O_3$ can be easily wet-etched, yet robust against interfacial reactions and moisture absorption. The uniqueness of ALD on III-V is so-called "self-cleaning effect", which is described in great details in Chap. 6.

The pre-cleaning or surface preparation before ALD is a very important process step to have a high-quality high-k/III-V interface, in particular, for GaAs. The simplified surface preparation for ALD on III-V developed by Ye et al. is following [79]. Before surface treatment, all wafers underwent standard degrease process using acetone, methanol and iso-propanol. The $NH_4OH$ treatment is carried out by soaking the samples in $NH_4OH$ (29%) solution for 3 min to remove native oxide and rinsing in flowing de-ionized (DI) water followed by gently drying the surface using $N_2$ blow-gun. The $NH_4OH$ etching step removes most of arsenic and gallium oxides from the surface. The further ALD process results on the disappearance of arsenic oxides and self-cleaning of GaAs surface [73, 83–86]. The interface quality could be further improved sometimes by $(NH_4)_2S$ treatment. The process is to soak the sample in $(NH_4)_2S$ for 10 min in room temperature and dry using $N_2$ gun. The effectiveness of $(NH_4)_2S$ passivation is mostly related with mono-layers of sulfur preventing further oxidation of III-V in ex-situ process. Most of sulfur is puffed off from III-V surface during the ALD process when the ALD chamber is heated to growth temperature of 300 °C. With these appropriate surface pretreatments, the interface trap density in the range of high $10^{11}$-low $10^{12}/cm^2$-eV can be realized and the inversion-type enhancement-mode MOSFETs can be demonstrated on GaAs, InGaAs and InP. During the past decades, the research community focused mainly on dielectric materials and III-V surface chemistry study, and paid less attention to device physics of III-V substrates. We emphasize that substrate is also extremely important as the second determinant for realizing a high inversion current as the proposed empirical mode describes below. This simple trap neutral level (TNL)-based empirical model can explain all experimental work on III-V MOSFETs using ex-situ ALD high-k dielectrics and also in-situ MBE-grown $Ga_2O_3(Gd_2O_3)$ gate dielectric.

A difficult problem with III-V MOSFETs results from the unpassivated dangling bonds on III-V free surfaces. The energy locations of the dangling bonds are directly related to the bulk band structures of different III-V semiconductors. But in the tight-binding formalism, the conduction and valence bands are formed as bonding and anti-bonding combinations of the atomic $sp^3$ hybrids. That is why the dangling-bond energy is typically located in the middle of the bandgap [107]. There are many experimental studies that quantitatively measure the midgap energies of various semiconductors. There are also dozens of theoretical models (such as metal induced gap state model, unified defect model, and disorder-induced gap state model) to quantitatively calculate the electronic energies. The historical evaluation of interface models is briefly summarized in Ref. [108]. The empirical model is rooted from the unified disorder induced gap state model (DIGS) proposed by Hasegawa and Ohno in 1986, which explains the striking correlation between the energy location $E_{min}$ for the minimum interface state density at the insulator-semiconductor interface and the Fermi level pinning position $E_{pin}$ of the metal-semiconductor interface. The central concept

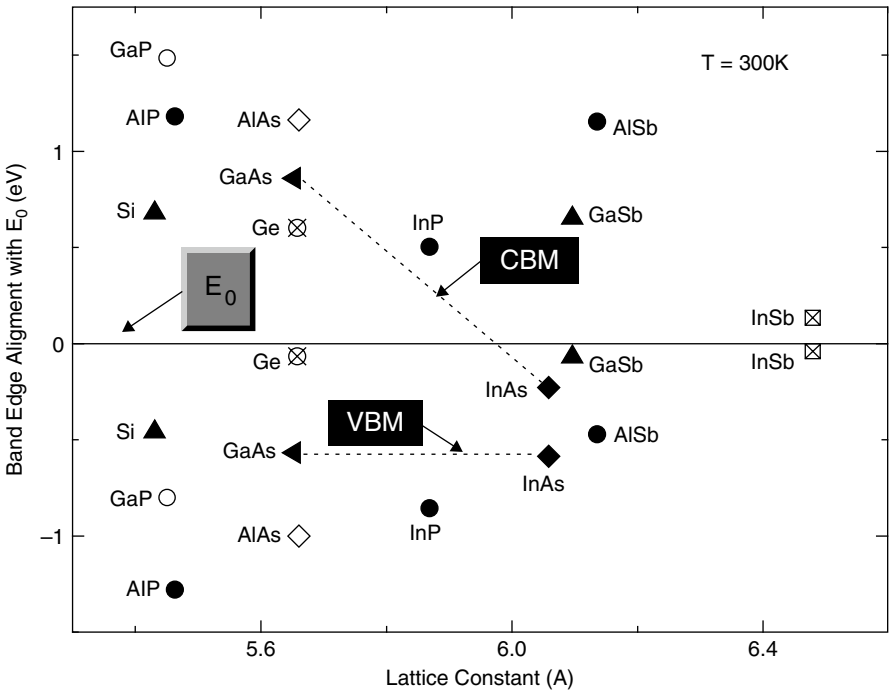


**Fig. 7.1** The energy alignment of the trap neutral level $E_0$ with the band edges of the representative semiconductors at MOS interfaces. The band edge values are obtained from Tiwari and Frank's Applied Physics Letters 60, 630 (1992). The *dashed lines* represent the rough CBM and VBM positions of $In_xGa_{1-x}As$

is that there is an energy level called trap neutral level $E_0$ at the high-k/GaAs or III-V interface,above which the trap states are of acceptor type or electron traps and below which are of donor type or hole traps. $E_0$ is at the same or similar energy level as $E_{min}$ and $E_{HO}$ in Ref. [29] and $E_{pin}$ at metal-semiconductor interfaces.

Figure 7.1 is the plot of several semiconductors' band edge alignment with the so-called trap neutral level ($E_0$) or Fermi level stabilization energy. In Si case, the state-of-the-art $SiO_2$/Si has low interface trap density of $10^9$–$10^{10}$/cm$^2$-eV. Although the energy separation between valence band maximum (CBM) and $E_0$ is ~0.6 eV and $E_0$ and valence band maximum (VBM) is ~0.5 eV, the density of trap states is low thus the Fermi-level is fully unpinned. Outstanding NMOSFETs and PMOSFETs are demonstrated and CMOS technology is widely applied. In Ge case, significant interface traps exist at various dielectrics/Ge interfaces though good progress was made in the past several years. PMOSFET in Ge is much easier to be realized compared to NMOSFET because $E_0$ is much closer to the valence band maximum (VBM) and far away from the conduction band minimum (CBM) [109, 110].

In the case of GaAs, $E_0$ is far away from both CBM and VBM so that both NMOSFET and PMOSFET in GaAs are difficult to realize if significant interface traps exhibit. If conduction band edge points of GaAs and InAs are connected, the CBM of

In-rich InGaAs is very near $E_0$. That's why inversion-mode InGaAs NMOSFETs could have high performance such as $G_m > 1.0$ S/mm and $I_{DS} > 1.0$ A/mm [90, 93]. The position of VBM of In-rich InGaAs is almost the same as that for GaAs or InAs. InGaAs PMOSFETs are expected to be difficult. In the case of GaSb, whose band alignment is so like Ge, a GaSb PMOSFET must be very easy to realize with good device performance according to the model.

## 7.4 Experiments on High-k/III-V MOSFETs

### *7.4.1 High-k/GaAs MOSFETs*

GaAs is the most studied III-V semiconductor in particular on (100) surface. A variety of devices are demonstrated and manufacturable on GaAs (100) surface such as GaAs HEMTs, LEDs and lasers. However, it is extremely difficult to realize Fermi level unpinning on this most useful surface with deposited oxide. GaAs inversion-mode or minority carrier devices on (100) surface mostly show minuscule drain current, indicating Fermi-level cannot be moved near or into CBM. We systematically study the electrical properties of inversion-mode NMOSFETs and PMOSFETs on GaAs (111)A, (111)B, (110) and (100) surfaces with ALD $Al_2O_3$ as gate dielectrics. (111)A is a pure Ga polar surface in contrast to (100) and (110) Ga-As non-polar surfaces, whilst (111)B is a pure As polar surface. The device work confirms that Fermi-level of GaAs (111)A surface is unpinned at the mid-gap with direct ALD $Al_2O_3$. The results obtained on GaAs (111)A surface are astonishingly different from those on GaAs (100), (110) and (111)B surfaces. The above proposed empirical model based on trap neutral level can explain the experimental observation. The XPS studies, in collaborations with UT Dallas, also confirm that Ga-oxide at $Al_2O_3$/GaAs (111)A interface is at detection limit in great contrast to what observed at GaAs (111)B, (110) and (100) surfaces [24].

MOSFET fabrication starts with 2-inch semi-insulating GaAs (111)A, (111)B, (110) or (100) substrates. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 30 nm thick $Al_2O_3$ layer was deposited at a substrate temperature of 300 °C as an encapsulation layer. Source and drain regions were selectively implanted with Si for NMOSFETs and Zn for PMOSFETs with the same dose of $5 \times 10^{14}$ cm$^{-2}$ at 40 keV through the 30 nm thick $Al_2O_3$ layer. Implantation activation was achieved by rapid thermal anneal (RTA) at 820 °C for 15 s in nitrogen ambient for NMOSFETs and at 750 °C for 15 s for PMOSFETs. An 8-nm $Al_2O_3$ film was regrown by ALD after removing the encapsulation layer by buffered oxide etch (BOE) solution and soaked in ammonia sulfide for 10 minutes for surface preparation. After 600 °C post-deposition anneal (PDA) in $N_2$ ambient, the source and drain ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Ni/Au for NMOSFETs or Pt/Ti/Pt/Au for PMOSFETs and a lift-off process, followed

by a RTA process at 400 °C for 30 s also in a $N_2$ ambient. The gate electrode was defined by electron beam evaporation of Ni/Au and a lift-off process. It was found during the process that GaAs (111)A surface is more hydrophilic like In-rich InGaAs surface and GaAs (100), (110) and (111)B surfaces are more hydrophobic. A hydrophilic surface is believed to be favorable for ALD two-dimensional growth and good interface properties.

A well-behaved I-V characteristic of a 4 μm-gate-length inversion-mode GaAs NMOSFET on (111)A surface is demonstrated in Fig. 7.2(c) with maximum drain current of 30 μA/μm, which is *a factor of 85000 or 25000 larger* than that obtained on (100) or (110) as shown in Fig. 7.2(a) and (b). Similar low inversion currents on GaAs (100) or (110) and even zero-current on GaAs (111)B lead to the conclusion of Fermi-level pinning in past reports. The GaAs (111)A surface is astonishingly different and Fermi-level is unpinned resulting in a large drain current. This astonishing difference can be partially explained by the empirical model as following.

By photoemission and other experiments, Spicer et al. discovered that $E_{pin}$ in GaAs is 0.75 and 0.5 eV above the valence band maximum (VBM)[111]. The first energy given is associated with a missing anion (As) and the second with a missing cation (Ga). Ignoring the complications of surface reconstructions, GaAs (111)A surface is a Ga-terminated polar surface, which can be regarded as a missing anion (As) surface with $E_0 = 0.75$ eV above VBM [111]. GaAs (100) is a Ga-As terminated surface which might be more related with missing cations with $E_0 = 0.5$ eV above VBM as shown in Fig. 7.3. The drain current strongly depends on the energy separation between $E_0$ and CBM for NMOSFET or VBM for PMOSFET. With the measured near mid-gap interface trap density $D_{it}$ of $2 \times 10^{12}/cm^2$ eV, the smaller the separation is, the less traps are filled in to prevent further Fermi level movement for strong inversion, the more inversion charge and drain current can be achieved. This model explains why NMOSFET on GaAs (111)A outperforms that on (100), and PMOSFET on GaAs (100) outperforms that on (111)A as reported in Ref. [35] that

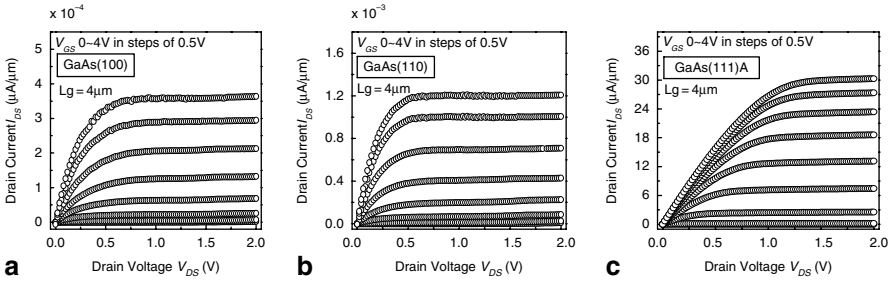


**Fig. 7.2** **a** Output characteristic ($I_{DS}$~$V_{DS}$) for $Al_2O_3$/GaAs(100) NMOSFET with 4 μm gate length. The maximum drain current is $3.5 \times 10^{-4}$ μA/μm. **b** Output characteristic ($I_{DS}$~$V_{DS}$) for $Al_2O_3$/GaAs(110) NMOSFET with 4 μm gate length. The maximum drain current is $1.2 \times 10^{-3}$ μA/μm. **c** Output characteristic ($I_{DS}$~$V_{DS}$) for $Al_2O_3$/GaAs(111)A NMOSFET with 4 μm gate length. The maximum drain current is 30 μA/μm

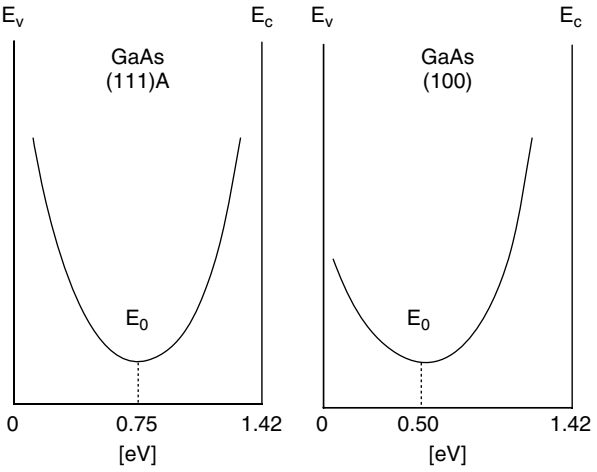


**Fig. 7.3** The Empirical model on GaAs. 0.75 eV is associated with a missing anion due to Ga (111)A surface; 0.5 eV is associated with a missing cation, which is the case most likely for (100) or (110). The minimum $D_{it}$ and U-shape curvature depends on processing conditions, while the location of $E_0$ remains constant for each semiconductor with the same crystal facet

shows that maximum drain current of 0.17 and 0.8 mA/mm are obtained on (111)A and (100) surfaces, respectively. Fermi-level pinning at the mid-gap of GaAs as proposed by the unified defect model (UDM) can be overcome by the appropriate surface preparation and the suitable dielectric deposition technique.

## 7.4.2 *High-k/$In_xGa_{1-x}As$ MOSFETs*

This empirical model is even valid in explaining the experimental data on high-k/$In_xGa_{1-x}As$ MOSFETs as shown in Fig. 7.4. The device structures and process are following. The channel is 15–20 nm thick $1 \times 10^{17}/cm^3$ doped p-type $In_{0.53}Ga_{0.47}As$

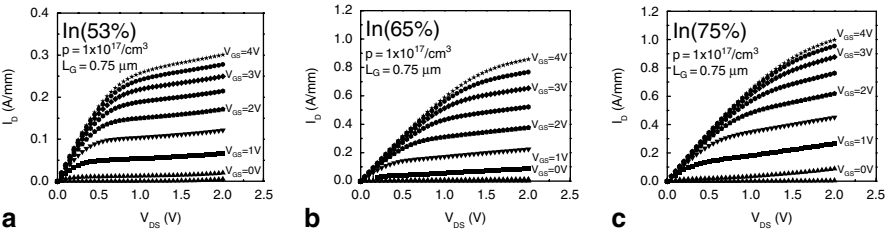


**Fig. 7.4** **a** Drain current ($I_D$) versus drain bias ($V_{DS}$) as a function of gate bias ($V_{GS}$) for $Al_2O_3$(8 nm) / $In_{0.53}Ga_{0.47}As$ NMOSFETs with 0.75-μm gate length. The maximum drain current is 0.3 A/mm. **b** Drain current versus drain bias as a function of gate bias for $Al_2O_3$ (10 nm)/$In_{0.65}Ga_{0.35}As$ NMOSFETs with 0.75-μm gate length. The maximum drain current is 0.86 A/mm. **c** Drain current versus drain bias as a function of gate bias for $Al_2O_3$(10 nm)/$In_{0.75}Ga_{0.25}As$ NMOSFETs with 0.75 μm gate length. The maximum drain current is 1.0 A/mm [91] (Reprinted with permission. Copyright 2008 IEEE)

or $In_{0.65}Ga_{0.35}As$ or $In_{0.75}Ga_{0.25}As$ channel layer, which is MBE epitaxially grown on $In_{0.53}Ga_{0.47}As$/InP substrate. 8–10 nm thick ALD $Al_2O_3$ is used as gate dielectric and Ni or Al is used as gate electrodes. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 30 nm thick $Al_2O_3$ layer was deposited at a substrate temperature of 300 °C as an encapsulation layer. Source and drain regions were selectively implanted with a Si dose of $1 \times 10^{14}\,cm^{-2}$ at 30 keV and $1 \times 10^{14}\,cm^{-2}$ at 80 keV through the 30 nm thick $Al_2O_3$ layer. Implantation activation was achieved by RTA at 700–800 °C for 10 s in a $N_2$ ambient. An 8–10 nm $Al_2O_3$ film was then re-grown by ALD after removing the encapsulation layer by BOE etching and ammonia sulfide surface preparation. After 400–600 °C PDA, the source and drain ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Ni/Au and a lift-off process, followed by a RTA at 400 °C for 30 s also in $N_2$ ambient. The gate electrode was defined by electron beam evaporation of Ni/Au and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 0.40 to 40 μm and a gate width of 100 μm. From transmission electron microscopy (TEM) images, no visible interfacial layer between $Al_2O_3/In_{0.75}Ga_{0.25}As$ interface and relaxation of $In_{0.75}Ga_{0.25}As$ on $In_{0.53}Ga_{0.47}As$ are observed. The native oxide of III-V material has been effectively removed by HCl etching, $NH_4OH$ and $(NH_4)_2S$ pretreatment and the ALD "self-cleaning" process.

Well-behaved I-V characteristic of 0.75-μm gate length inversion-type E-mode $In_{0.53}Ga_{0.47}As$, $In_{0.65}Ga_{0.35}As$ and $In_{0.75}Ga_{0.25}As$ NMOSFETs are demonstrated in Fig. 7.4 with the $I_{DMAX}$ of 0.3, 0.86 and 1.0 A/mm, respectively. The gate leakage current ($I_G$) is less than $10^{-4}\,A/cm^2$ at 4.0 V gate bias ($V_G$) for all devices. The extrinsic $G_m$, the intrinsic $G_m$, and the threshold voltage $V_T$ for $In_{0.75}Ga_{0.25}As$ NMOSFETs are 0.43 S/mm, 0.52 S/mm, and 0.5 V, respectively, with 0.75-μm gate length. The $I_{DMAX}$ and $G_m$ increase with increasing indium content in InGaAs not only due to the increase of mobility and saturation velocity and reduced contact resistance. More importantly, according to Fig. 7.1, TNL level $E_0$ in $In_{0.75}Ga_{0.25}As$ is much near CBM than $In_{0.53}Ga_{0.47}As$. The inversion charge and inversion current on $In_{0.75}Ga_{0.25}As$ MOSFET is much larger than those on $In_{0.53}Ga_{0.47}As$ MOSFET as demonstrated experimentally in Fig. 7.4. In general, In-rich InGaAs has much smaller energy separation between TNL and CBM, compared to GaAs. Less acceptor traps are filled by inversion in In-rich InGaAs. The inversion charge density realized in In-rich InGaAs is much more than that in GaAs. That's why the on-state performance for In-rich InGaAs MOSFETs is better than that for GaAs MOSFETs.

With more demonstrated on-state performance of inversion-mode MOSFETs on In-rich InGaAs channels, more work are needed to study the fundamental limitation of narrow energy gap of In-rich InGaAs and the off-state performance related with exhibiting interface trap densities. For example, recent works unveil that the interface traps at ALD $Al_2O_3$/InGaAs interface are mostly donor-type with so far measured lowest $D_{it}$ from $8.0 \times 10^{11}/cm^2\,eV$ to $2.0 \times 10^{12}/cm^2\,eV$ near the conduction band edge and increases continuously to $\sim 10^{13}/cm^2\,eV$ level at the valence band edge [112]. Further reducing the interface traps to the required device quality level is essential and remains a big challenge in III-V MOS field.

### 7.4.3 High-k/InP MOSFETs

Although InP is a commonly used compound semiconductor with wide applications in electronic, optoelectronic, and photonic devices, high-k dielectric integration on InP is largely unexplored. Compared to GaAs, InP is widely believed to be a more forgiving material with respect to Fermi level pinning and has a higher electron saturation velocity ($2 \times 10^7$ cm/s) as well. Detailed Monte-Carlo simulations of deeply scaled n-MOS devices indicate that an InP channel could enable high-field transconductance ~60% higher than either Si, Ge, or GaAs at equivalent channel length [113]. It could be a viable material for high-speed logic applications if a high-quality, thermodynamically stable high-k dielectric could be found. In the few reported works on InP MOSFETs since the 1980s, $SiO_2$ was primarily used gate dielectric and devices suffered from significant current and threshold voltage drift due to the poor semiconductor-dielectric interface [114, 115]. Although Fermi-level unpinning was achieved through applying appropriate surface treatment before $SiO_2$ deposition, current and effective channel mobility remained low and interface trap density was far from applicable [116–119]. By implementing ALD high-k dielectrics on InP, we are able to revisit this historically unsolved problem and demonstrate Fermi level unpinning of InP surface with ALD high-k dielectrics. More importantly, InP as a different material from $In_xGa_{1-x}As$ (x from 0 to 1 including GaAs and InAs) series is an appropriate test for the validity of the proposed empirical model.

The starting material for an ALD high-k/InP MOSFET fabrication is an InP semi-insulating substrate with Fe as deep level traps [120]. After surface degreasing and $(NH_4)_2S$-based pretreatment, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 30 nm thick $Al_2O_3$ layer was deposited at a substrate temperature of 300 °C, using alternately pulsed chemical precursors of $Al(CH_3)_3$ (the Al precursor) and $H_2O$ (the oxygen precursor) in a carrier $N_2$ gas flow. Source and drain regions were selectively implanted with a Si dose of $1 \times 10^{14}$ cm$^{-2}$ at 140 keV through the 30 nm thick $Al_2O_3$ layer. Implantation activation was achieved by RTA at 720 °C for 10 s in a nitrogen ambient. The $Al_2O_3$ encapsulation layer was removed by HF and $Al_2O_3$ or $HfO_2$ gate dielectrics were grown by ALD again with the thickness between 4 and 10 nm. The source and drain ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Pt/Au and a lift-off process, followed by a RTA process at 500 °C for 30 s also in a $N_2$ ambient. The gate electrode was defined by electron beam evaporation of Ti/Au and a lift-off process. The fabricated MOSFETs have a nominal gate length varying from 0.75 to 40 μm and a gate width of 100 μm.

A well-behaved I-V characteristic of an E-mode InP NMOSFET with 10 nm $HfO_2$ as gate dielectric is demonstrated in Fig. 7.5(a) with maximum drain current over 100 mA/mm at $V_{ds}$ = 3V and $V_{gs}$ = 4V. The device was simply fabricated on semi-insulating InP (100) substrate. The device is off at $V_{gs}$ = 0V without significant drain-source leakage current or substrate current due to the high bandgap of InP. In general, it is surprised to obtain 100 mA/mm level drain current on InP substrate since only a few hundreds of μm/mm drain current was observed on GaAs (100)

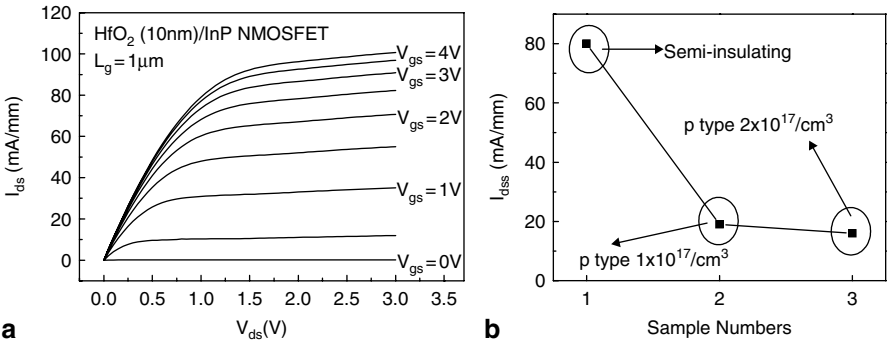


**Fig. 7.5** **a** *I–V* characteristic of a 1.0 μm gate length InP MOSFET with a 30 nm ALD $HfO_2$ as a gate dielectric. **b** Comparison of maximum drain current with different InP channel doping concentration with $Al_2O_3$ as gate dielectric. Current in Sample 2 and Sample 3 is lower than that in Sample 1

without ICL layer. We ascribe it to the fact that the energy separation between CBM and TNL for InP is 0.5 eV instead of 0.8 eV for GaAs (100). This makes it easier for InP to realize inversion, compared to GaAs (100). Meanwhile, the energy separation between CBM and TNL for $In_{0.53}Ga_{0.47}As$ is ~0.2 eV and for $In_{0.75}Ga_{0.25}As$ is <0.1 eV. That's why $In_{0.53}Ga_{0.47}As$ MOSFET and $In_{0.75}Ga_{0.25}As$ MOSFET deliver much more drain currents than InP MOSFET. InP data further proves the validity of the empirical model for high-k/III-V MOSFETs. Similar devices were also fabricated on MOCVD grown InP epi-wafers with p-type doping concentration of $1 \times 10^{17}/cm^3$ and $2 \times 10^{17}/cm^3$. The maximum drain current drops to 17 mA/mm for p type $2 \times 10^{17}/cm^3$ channel and 20 mA/mm for $1 \times 10^{17}/cm^3$ channel as shown in Fig. 7.5(b). The result is consistent with what is observed in InGaAs MOSFETs [89]. The qualitative understanding of this observation is that more surface bending is required for high doping channels to realize strong inversion condition. In other words, for p-type doped InP, Fermi-level is located near the valence band maximum. If the Fermi-level and TNL is aligned at the first place, more negative charges are built in at the interface which makes further inversion more difficult.

### *7.4.4 High-k/GaSb MOSFETs*

The modern microelectronic industry is built up on a Si-based CMOS technology in order to control the power assumption. CMOS technology requires high-performance NMOSFET and PMOSFET. Although significant progress was made in the past years on high-k/III-V integration, there are few breakthrough results on III-V PMOSFETs, compared to III-V NMOSFETs. One exception is Intel's p-channel InSb quantum well transistors [103]. However, this approach is hard to integrate in large scale due to the large gate current leakage. The issues and progress on III-V PMOSFET are reviewed in Chap. 12 in this book [121, 122]. An ultimate CMOS approach, yet to be demonstrated, is to use InGaAs as NMOSFET channel and

Ge as PMOSFET channel, and integrate both on Si CMOS platform. The cross contamination between III-V and Ge might be a big hassle for this approach. Here, we discuss the fundamental advantage of using GaSb as p-channel material for the potential full III-V CMOS technology in accordance with the empirical model. The principle of physics is supported by the preliminary results on ALD $Al_2O_3$/GaSb material system with C-V characterization of MOSCAPs and I-V characterization of PMOSFETs.

GaSb has a bandgap of 0.7 eV. GaSb is lattice-matched to InAs. GaSb could be epitaxially grown on In-rich InGaAs with controllable strain and eventually heterogeneously integrated on Si CMOS platform. Compared to Ge, GaSb doesn't have cross contamination issue with In-rich InGaAs. Hole mobility of GaSb is ~800 $cm^2$/Vs much higher than most of other III-V materials though lower than that of Ge (1900 $cm^2$/Vs). However, the limitation of current in inversion-mode alternative channel MOSFETs is not the mobility but the inversion charge density. For example, GaAs (100) has 8000 $cm^2$/Vs electron mobility in bulk and its inversion-mode MOSFETs show very low drain current with directly deposited high-k dielectrics. That's because it's hard to realize strong inversion charge density in GaAs with interface traps. This important understanding of non-Si MOS interfaces has been highlighted in Fig. 7.1. In the case of GaSb, whose band alignment is so like Ge, GaSb PMOSFET must be very easy to realize with good device performance.

N-type GaSb substrate with doping concentration of $5 \times 10^{17} cm^{-3}$ are used for MOSCAPs and MOSFETs study. After degreasing by acetone and methanol and pre-cleaning by HCl:$H_2O$ = 1:1 for 30 s to etch away native oxide and $NH_4OH$ for 60 seconds to remove elemental Sb [123], 8 nm $Al_2O_3$ was deposited at 300 °C in ASM F-120 ALD reactor. Ni is used as metal electrode for MOSCAPs. GaSb PMOSFETs were fabricated as following. 30 nm ALD $Al_2O_3$ served as an encapsulation layer and source and drain were Zn implanted at 40 KeV and $1 \times 10^{14}/cm^2$. 8 nm $Al_2O_3$ was re-grown, followed by 600 °C 45 s PDA in $N_2$ ambient for dopant activation. Ti/Pt/Au were used as Ohmic metal contacts and annealed at 400 °C by RTA. Ni/Au were used as metal gate. From the multi-frequency CV plots from 1 KHz to 1 MHz on Ni/$Al_2O_3$/GaSb MIS structure, although large frequency dispersion at accumulation side may indicate significant interface traps exhibiting, nevertheless, it does not inhibit the approach of inversion, seen in Fig. 7.6(a). As illustrated in Fig. 7.1 for GaSb, the $E_0$ is close to VBM and only traps located between $E_0$ and VBM decide the final inversion. Hole inversion is easy for GaSb, similar to Ge. Figure 7.6(b) shows the I-V characteristics of a 0.75 µm-gate-length GaSb PMOSFET with drain current 1.7 µA/µm. It proves the inversion can be achieved in GaSb at transistor level, though the drain current is much smaller than its counterpart Ge. The newest result shows that drain current of a 0.75 µm GaSb PMOSFET increases to 70 µA/µm with refined Si implanted source and drain. These on-state performances should be possible further improved with optimizing ALD growth condition and device fabrication process. The preliminary results on GaSb further confirms that the empirical model works quite general on all III-V semiconductors including GaSb.

The empirical model is also valid for other III-V materials such as InAs [124], InSb [102, 125] and GaN [126–128]. Our experiments, along with the results from

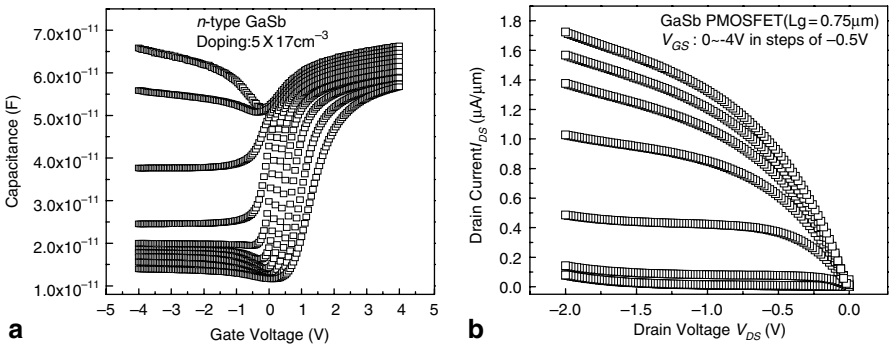


**Fig. 7.6** **a** $C-V$ plots on Ni/$Al_2O_3$/n-GaSb structure from 1 KHz to 1 MHz with 10 points. Large frequency-dispersion is observed at accumulation side, however, inversion characteristics can still be achieved due to that $E_0$ is close to $E_V$ or VBM as illustrated in Fig. 7.1. **b** Output characteristic ($I_{DS}$~$V_{DS}$) for GaSb PMOSFET with 0.75 μm gate length. The maximum drain current is ~1.7 μA/μm

other leading groups in the field, verify this statement. The conclusion is that with decent interface quality as the pre-condition, the energy separation between TNL and CBM is the most important determinant for high-performance inversion-mode NMOSFETs and the energy separation between TNL and VBM for PMOSFET.

## 7.5 Conclusion

The quest for practical GaAs MOSFETs started in early 1960's has been continued in the 21st century with many work focused on ALD high dielectrics. We briefly reviewed the history over the past 40 years and current status of III-V MOSFET research to help those new in the field to have easy access to the many existing publications. We use an empirical model based on the TNL concept to explain all reported experimental observations on inversion-type enhancement-mode ALD high-k/III-V MOSFETs and MBE $Ga_2O_3(Gd_2O_3)$/III-V MOSFETs reported by M. Hong et al. Although the origin of this empirical model can be tracked back to the Hasegawa's DIGS model, this is the first time that we have systematically surveyed various III-V substrates and demonstrated the validity of the model. It is based on experimental demonstration of inversion-mode MOSFETs so that we call it "empirical model". The studied high-k/III-V interfaces include GaAs, $In_xGa_{1-x}As$, InAs, InP, InSb, GaN and GaSb. With ALD high-k dielectrics, in particular the most studied $Al_2O_3$, the interface quality with $D_{it}$ between low $10^{11}$-low $10^{12}$/cm$^2$ eV is significantly improved from previous work in 1970s and 1980s. Fermi-levels on GaAs (111)A, In-rich InGaAs, InP, GaSb, and others are not pinned. Inversion-mode MOSFETs on different III-V substrates can be demonstrated as shown in Sect. 7.4. However, the validity of this empirical model also tells us the interface quality is far from ideal such as $D_{it}$ of $10^9$–$10^{10}$/cm$^2$ eV as $SiO_2$/Si interface. Much

work is still needed to make high-k/III-V research become a manufacturable III-V CMOS technology.

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