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Performance and Variability Studies of InGaAs Gate-all-around Nanowire MOSFETs

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***Abstract*—Furthering Si CMOS scaling requires development of high-mobility channel materials and advanced device structures to improve the electrostatic control. We demonstrate the fabrication of gate-all-around (GAA) InGaAs MOSFETs with highly scaled atomic-layer-deposited (ALD) gate dielectrics. InGaAs, with its high electron mobility, allows higher drive currents and other on-state performance compared to silicon. The GAA structure provides superior electrostatic control of the MOSFET channel with outstanding off-state performance. A subthreshold slope of 72 mV/dec, electron mobility of 764 cm^2/V s, and an on-current of 1.59 mA/μm are demonstrated, for example. Variability studies on on-state and off-state performances caused by the number of nanowire channels are also presented.**

***Index Terms*—Gate-all-around, nanowire, InGaAs, MOSFET**

I. Introduction

III-V compound semiconductors has recently drawn wide interest in the device community for its potential application in future CMOS technology as channel materials [1]. Among various III-V materials under consideration, Indium Gallium Arsenide (InGaAs) is considered one of the most promising materials for N-channel MOSFETs, due to its high electron mobility, high electron velocity, and unique band alignment. Various high-*K* dielectric integration schemes and interface passivation techniques have been investigated to improve high-*K*/InGaAs interface quality and achieve sub-1nm equivalent-oxide-thickness (EOT) [2-7]. On the other hand, to meet the scaling requirements at sub-10nm technology node, non-traditional device structure such as ultra-thin body and multiple-gate structure is strongly needed. Indium-rich InGaAs materials intrinsically have smaller bandgap, larger permittivity, and smaller effective mass, which make them even more susceptible to short channel effects. III-V-on-insulator structure with extremely thin (<10nm) body thickness has been demonstrated by wafer-bonding technique [8] and epitaxial transfer method [9]. In the mean time, InGaAs FinFETs with surface and buried channel has been proposed and demonstrated. Improved scalability has been confirmed with FinFET structure against planar and thin-body structure [10-12]. In the category of multiple gate devices, the gate-all-around (GAA) nanowire MOSFETs is the most promising option in terms of electrostatic control. High performance Si GAA nanowire devices have been demonstrated and its operating principle studied comprehensively [13-18]. Recently, a novel top-down fabrication technology has been developed and sub-50nm InGaAs GAA nanowire MOSFETs has been demonstrated [4, 7, 19]. Scalability and variability improvements has been obtained by aggressive EOT scaling and interface passivation [20]. In this paper, the device performance for InGaAs GAA nanowire MOSFETs with various gate stack, nanowire size, and interface passivation has been summarized, with a particular focus on device variation aspects. The paper is organized as follows: Part II provides details of fabrication process and summarizes different samples under investigation. Part III and VI study the channel length (L_{ch}), nanowire size, and interface dependency for device on-state and off-state performance, respectively. Part V describes intrinsic device parameters, including the effective channel mobility. Part VI describes the unique variability induced performance shift in nanowire transistors.

This work was supported in part by the U.S. National Science Foundation, the Semiconductor Research Corporation Focus Center Research Program Materials, Structures, and Devices Focus Center, the Air Force Office of Scientific Research monitored by Prof. J.C.M. Hwang.

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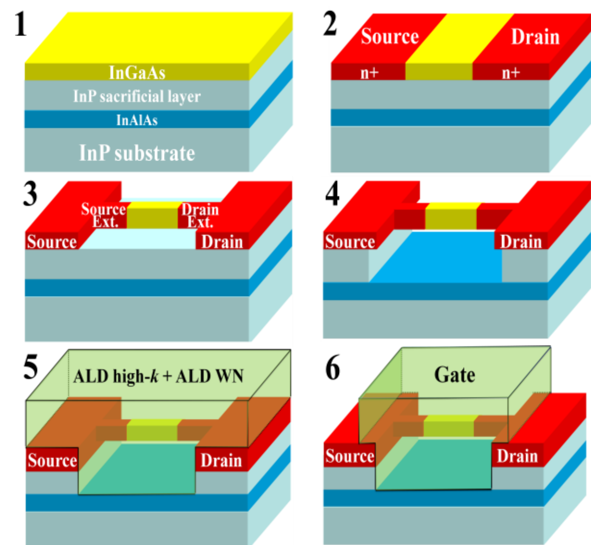

Fig. 1. Schematic view and key fabrication processes for InGaAs GAA FETs.

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II. Device Fabrication

Figure 1 shows a schematic view and the key fabrication processes for InGaAs GAA FETs. The starting material is InGaAs channel layers on (100) InP substrate (Figure 1-1). After $(NH_4)OH$ pretreatment, a 10nm ALD Al_2O_3 was deposited as an encapsulation layer. Source/drain implantation (Si: 20keV/$1\times10^{14}cm^{-2}$) was then performed, using PMMA resist as mask. The smallest channel length L_{ch} defined was 20nm (Figure 1-2). Dopant activation was done by rapid thermal annealing at 600°C for 15 seconds in N_2 ambient. Then InGaAs fin structures were defined by ICP plasma etching (BCl_3/Ar) (Figure 1-3). The diluted ZEP520A resist (100nm) was used as etching mask. The smallest nanowire width (W_{NW}) defined was 20nm. Then localized nanowire release process was carried out using diluted HCl solution (Figure 1-4). HCl based solution can selectively etch InP over InGaAs. However, the etching is found to be highly anisotropic. Therefore the InGaAs fins have to be patterned along <100> directions for a successful release process. After BOE and diluted HCl:H_2O_2 clean, the samples were soaked in 10% $(NH_4)_2S$ for 10 minutes. Then high-k dielectric/WN metal gate were grown by ALD surrounding the nanowire channel as gate stack (Figure 1-5). WN was grown at temperature of 385°C. Bis(tert-butylimido)bis(dimethylamido)tungsten(VI) vapor and ammonia gas were use as the WN precursors. The sheet resistance of the ALD WN film was measured by a four-point probe station, and the resistivity was 2.2 Ω·cm for a 40 nm WN film. Cr/Au gate pattern were then defined and used as hard mask for the following gate etch using CF_4/Ar ICP plasma etching. The gate pattern has 50nm overlap region over source/drain implanted area beyond the nanowire, as shown in Figure 1-6, due to the non-self-aligned process. Source/drain metal was then formed by e-beam evaporation of Au/Ge/Ni and annealing at 350°C. Cr/Au test pad definition concludes the fabrication process (Figure 1-6). Table I summarizes the samples fabricated and characterized in this paper.

TABLE I

Sample	Channel material	L_{ch} (nm)	W_{NW} (nm)	T_{NW} (nm)	Gate oxide	EOT (nm)	No. of wires
IEDM11	$In_{0.53}Ga_{0.47}As$	50-120	30-50	30	10nm Al_2O_3	4.5	1, 4, 9, 19
IEDM2012 (Sample A Al_2O_3-first)	$In_{0.65}Ga_{0.35}As$	20-80	20-35	30	0.5nm Al_2O_3/ 4nm $LaAlO_3$	1.2	4
IEDM2012 (Sample B $LaAlO_3$-first)	$In_{0.65}Ga_{0.35}As$	20-80	20-35	30	4nm $LaAlO_3$/ 0.5nm Al_2O_3	1.2	4
IEDM2012 (Sample C)	$In_{0.65}Ga_{0.35}As$	20-80	20-35	30	3.5nm Al_2O_3	1.7	4
InGaAs GAA MOSFET (Unpublished Work)	$In_{0.65}Ga_{0.35}As$	20-80	20-35	30	5nm Al_2O_3	2.2	4
Ultrathin InGaAs GAA MOSFET	$In_{0.65}Ga_{0.35}As$	20-80	20-30	6	5nm Al_2O_3	2.2	4

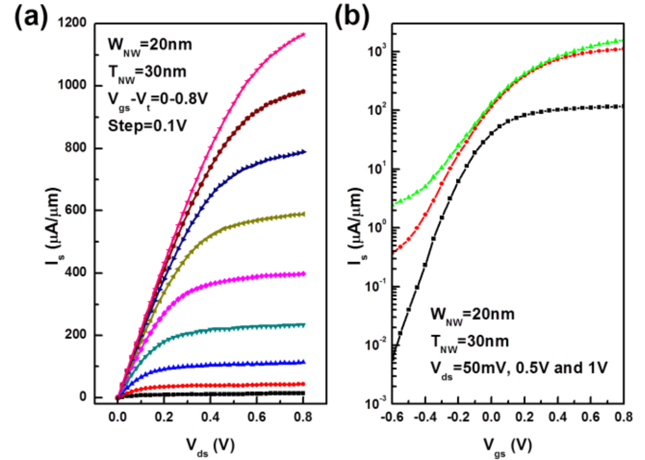

Fig. 2 (a) Output and (b) transfer characteristics of the device with the largest saturation source current 1.59 mA/μm at V_{ds}=1V.

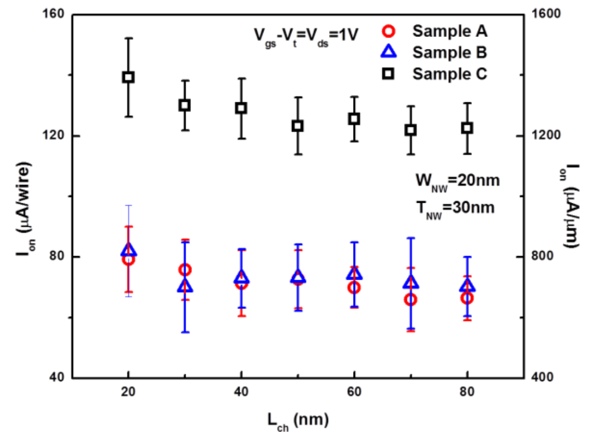

Fig. 3. I_{on} scaling metrics of InGaAs GAA MOSFETs with three gate stacks.

III. On-State Performance of the InGaAs GAA MOSFET

In this section, we discuss the key factors in the on-state performance of the InGaAs GAA MOSFETs. We have demonstrated three ways to improve the on-state performance of InGaAs MOSFET: channel length, nanowire dimension, and EOT scaling.

A. Channel length scaling

The InGaAs GAA MOSFET has excellent immunity to short channel effect which enables us to continue the channel length scaling down to 20nm. The extremely short channel enables us to obtain saturation current as high as 1.59 mA/mm at V_{ds}=1V in an InGaAs GAA MOSFET with 20nm channel length, 20nm wire width, 30nm wire thickness and 1.7nm EOT. Figure 2 shows the well-behaved output and transfer characteristics of this deep sub-100nm nanowire device.

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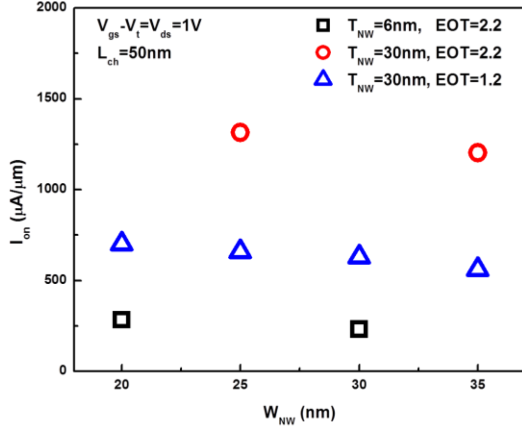

Fig. 4. Effect of nanowire dimension W_{NW} on the on-current.

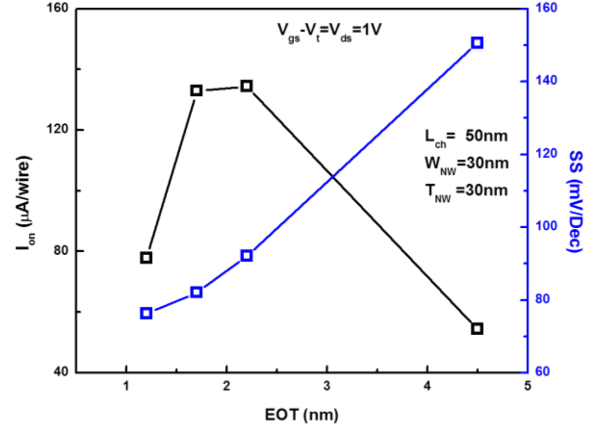

Fig. 5. Effect of EOT scaling on the on-currents of different devices.

Channel length scaling is an effective way to improve the on-current in long channel devices because the saturation current is inversely proportional to the channel length. However, with the channel length step into sub-100nm regime, I_{on} scaling saturates. Figure 3 shows the on-current scaling metrics of the InGaAs GAA MOSFETs with different gate stacks. Samples A and B have a 0.5nm Al_2O_3/4nm $LaAlO_3$ stack (EOT = 1.2nm), where Al_2O_3 was grown before $LaAlO_3$ for Sample A and vice versa for Sample B. Sample C has 3.5nm Al_2O_3 gate (EOT = 1.7nm). The saturation current increases very slowly in the sub-100nm regime by decreasing channel length. The reasons are two-folds: On the one hand, velocity saturation limits the velocity of the electron at high electric field [21]. In short channel devices, the strength of the electrical field is so high that the velocity of electron almost stays at the same with different channel lengths so as to the saturation current. On the other hand, statistical law in electron transportation doesn't work in extremely short channel devices. The short channel devices may work in a near ballistic regime. The electron in the channel is likely to transport from source to drain without scattering or only scatter for a few times. In this case, the current of the device depends more on the contact of the transistor rather than the channel length. When totally ballistic transport is obtained, the current only depends on the contact resistance [22].

B. Nanowire dimension optimization

InGaAs GAA MOSFET has a relatively larger drive current, comparing to other device structures such as planar structure and FinFET structure because of the better gate control. Simulation works have shown that the channels of InGaAs GAA MOSFETs are volume inverted which explains the fact that devices with smaller nanowire structures show larger normalized on-current [23].

We have systematically studied the dimension dependency of the on-currents. Devices with 20-35 nm nanowire width (W_{NW}) and 6nm or 30nm nanowire thickness were fabricated and the dependence of on-current with the geometrical dimension of the transistor is presented in Figure 4. It is found that the on-current keeps increasing with nanowire dimension scaling from 35nm to 20nm, consistent with simulation work. However, devices with 6nm nanowire thick have relatively low current. The reason is that surface roughness has more significant effect on the mobility of the InGaAs channel than volume inversion when the channel is down to 6nm level. Because the nanowire is so thin, electrons are more likely to scatter at the surfaces and mobility is degraded.

C. EOT scaling

It is well known that the on-current of a MOSFET is proportion to the gate capacitance (C_{ox}) at the same drain and gate biases and C_{ox} is inversely proportional to the equivalent gate oxide thickness (EOT). Thus, it is an effective way to improve the on-current at the same bias conditions by scaling EOT.

Here, InGaAs GAA MOSFETs with EOT=4.5nm (10nm Al_2O_3), EOT=2.2 (5nm Al_2O_3), EOT=1.7 (3.5nm Al_2O_3), and EOT=1.2 (0.5nm Al_2O_3/4nm $LaAlO_3$) are used to compare the on-current with different EOTs. Figure 5 shows the relationship between the on-current and the EOT. Theoretically, I_{on} and EOT should form a straight line in the plot. However, we found that the curve resembles a parabola with a peak at around 2nm. The reason is that with EOT scaling down, remote scattering from the oxide layer such as Coulomb scattering, becomes larger. Therefore, the mobility of devices with a smaller EOT is degraded, compared to a larger EOT device[24]. As a result, the currents of the devices with an EOT less than 2nm are decreased.

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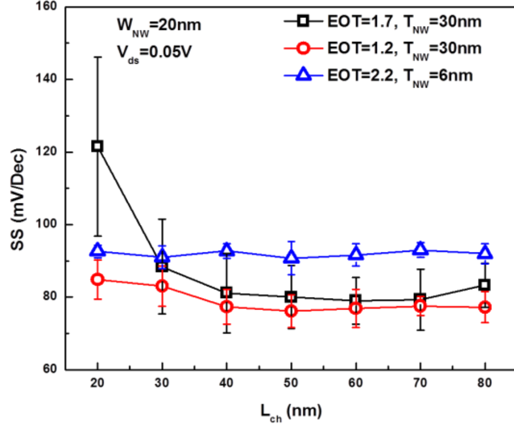

Fig. 6. SS channel length scaling metrics for different EOT and nanowire dimensions.

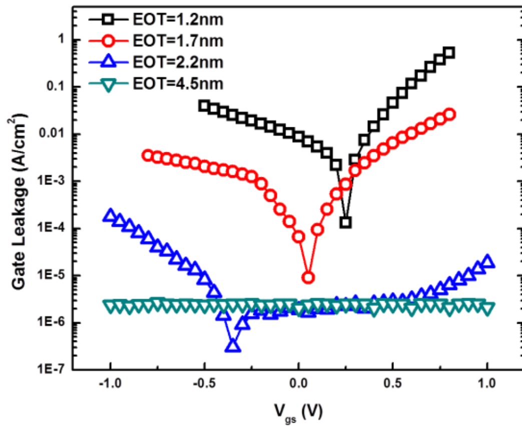

Fig. 7. Relationship between EOT and gate leakage current.

IV. OFF-STATE PERFORMANCE OF THE INGAAS GAA MOSFET

One of the scalability bottlenecks of planar MOSFETs is the short channel effect. Excellent immunity to short channel effect is another benefit of the InGaAs GAA MOSFETs. In this section, we mainly focus on the experimental evidence on how significant the GAA structure can reduce the short channel effect of the InGaAs MOSFETs. Generally, there are three ways to improve the off-state performance: EOT scaling, nanowire dimension shrinkage, and interface engineering.

A. *EOT scaling*

One of the most straightforward ways to improve the off-state performance is to reduce the EOT. Lower EOT leads to better electrostatic control and in turn, smaller SS and DIBL. Figure 5 shows the relationship between EOT and SS using devices with L_{ch}=50nm, W_{NW}=30nm and T_{NW}=30nm. We can see clearly that devices with lower EOT have better off-state performance. Figure 6 shows the comparison of SS between two group of devices with EOT=1.2nm and EOT=1.7nm and 30nm wire thickness. We can find that devices with

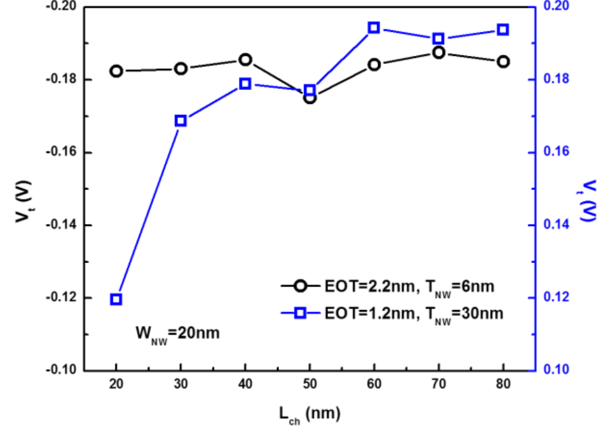

Fig. 8. Channel length scaling metrics for threshold voltage.

EOT=1.2nm have a much smaller SS and almost no increase with channel length scaling down to 20nm.

We have seen that EOT scaling is an effective way to improve the off-state performance. However, keeping push EOT down to 1nm or less is still challenging. Figure 7 shows the relation between gate leakage current and EOT. Leakage current increases very fast with EOT scaling down. Theoretically, the gate leakage current has an exponential relationship with gate insulator thickness. That is why high-k material ($LaAlO_3$, k~25) is used in this work. As described in the previous section, carrier mobility in the channel could also be degraded with aggressively scaled EOT.

B. *Nanowire dimension scaling*

Another way to improve the off-state performance is to reduce the dimension of the nanowire so that better gate control can be achieved. As shown in Figure 6, the devices with EOT=2.2nm and 6nm thick nanowire show no SS increase with channel length scaling which means the ultrathin device has better immunity to short channel effect. Meanwhile, the devices with EOT=1.2nm and 1.7nm and T_{NW}=30nm show the increase of SS when the channel is 40nm or less.

As shown in Fig. 6, the device with T_{NW}=6nm shows the largest SS in the long channel regime. The reason is that SS not only depends on the immunity to short channel effect but also depends on the interface trap density (D_{it}). Without taking short channel effect into account, the SS can be expressed as $SS=60(1+qD_{it}/C_{ox})$. The higher the D_{it} is, the larger the SS. By EOT scaling, C_{ox} can be increased and therefore the effect of interface trap on SS is reduced.

Figure 8 shows the V_t comparison between the device with EOT=2.2nm, T_{NW}=6nm and the device with EOT=1.2nm, T_{NW}=30nm, both of them have the same nanowire width, linear extrapolation method is used in V_t extraction. It can be seen clearly that V_t rolls off in device with EOT=1.2nm, T_{NW}=30nm; however, V_t remains the same in device with EOT=2.2nm, T_{NW}=6nm. The V_t roll-off verifies that those devices with EOT=1.2nm and T_{NW}=30nm are still strongly affected by the short channel effect at channel length of 50 nm or less, while

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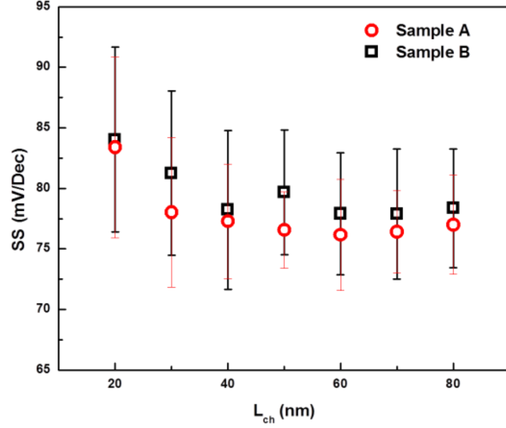

Fig. 9. SS comparison between devices with different gate stack at EOT=1.2nm, T_{NW}=30nm and W_{NW}=20nm. Samples A and B have a 0.5nm Al_2O_3/4nm $LaAlO_3$ stack (EOT = 1.2nm), where Al_2O_3 was grown before $LaAlO_3$ for sample A and vice versa for sample B. Sample A has a better interface than Sample B.

the ultrathin 6nm nanowire devices have better immunity to short channel effect.

Therefore, in short channel InGaAs nanowire devices, both interface trap and short channel effects can degrade the off-state performance. EOT scaling improves the off-state performance by providing better gate control and reducing the effect of D_{it} with increased gate capacitance. On the other hand, the nanowire dimension scaling can improve the off-state performance only by providing better gate control to reduce the short channel effect. The ultrathin nanowire structure gives a better immunity to short channel effect than EOT scaling.

C. Interface Engineering

Interface trap density is one of the factors that degrade the off-state performance as discussed above. Figure 9 compares devices with different gate stack thus with different D_{it}. We found that the 0.5nm Al_2O_3/4nm $LaAlO_3$ stack has a lower average SS than the 4nm $LaAlO_3$/0.5nm Al_2O_3 stack. Thus, it is confirmed that a better interface quality can be obtained with thin Al_2O_3 layer insertion between high-k $LaAlO_3$ and InGaAs.

V. Effective Mobility

The on-state performance of a device is strongly correlated to the mobility of the channel semiconductor. Although electron mobility (μ_n) of bulk InGaAs is ~10^4 cm^2/V s, the mobility is reduced considerably for a fully process GAA transistor, due to non-ideal effects such as series resistance and interface scattering. These effects must be de-embedded from measured data in order to determine the true performance of the InGaAs GAA MOSFET.

Here, we pursue for extraction of intrinsic effective mobility of InGaAs nanowire channels by fitting measured data to a MOSFET model based the BSIM3 Unified I-V Model [25]. The BSIM model does not fit the nanowire characteristics in the deep-subthreshold region where drain to source leakage has a significant effect. An extra drain to source leakage term, $I_{leak,V_{ds}}$, is added to the model. Since the magnitude of leakage is dependent on the drain voltage, its value must be extracted for each V_{ds} measured. With this extra parameter, the model fits the nanowires in the low V_{ds} region ($V_{ds} \lesssim 2v_t$) very well, even though it was designed for planar silicon devices.

The core of the low-V_{ds} model is a formula for an effective gate to source voltage (V_{gsteff}):

$$V_{gsteff} := \frac{2nv_t \ln\left[1 + \exp\left(\frac{V_{gs}' - V_t}{2nv_t}\right)\right]}{1 + 2nC_{ox}\frac{v_t}{Q_0}\exp\left(-\frac{V_{gs}' - V_t}{2nv_t}\right)}$$

where n is the subthreshold swing parameter, v_t is the thermal voltage kT/q, V_{gs}' is the intrinsic gate voltage and equals $V_{gs} - I_s R_s$, R_s is assumed to be half of series resistance R_{ds}, V_t is the threshold voltage and is dependent on V_{ds} because of short channel effects, C_{ox} is the gate to channel capacitance, and Q_0 is the charge in the channel at threshold [25].

The use of V_{gsteff} allows a simple equation to be used for calculating the device current in both the subthreshold and strong inversion regions. V_{gsteff} is approximately ($V_{gs} - V_t$) in the strong inversion region and $(Q_0/C_{ox})\exp[(V_{gs}' - V_t)/nv_t]$ in the subthreshold region. Incorporating $I_{leak,V_{ds}}$ and R_{SD}, allows the following to be used to implicitly solve for I_S:

$$I_S = \frac{W}{L}\mu C_{ox} V_{gsteff}(V_{ds} + I_S R_{SD})$$

W is the device width, L is the channel length, and I_S is the source current [25]. The device width is taken to be the circumference of the wires and C_{ox} is calculated based on the oxide material and its thickness.

The device mobility μ is modeled as:

$$\mu := \frac{\mu_0}{1 + \theta_1(V_{gsteff}) + \theta_2(V_{gsteff})^2}$$

This formula describes how increasing the gate to channel electric field causes the mobility to decrease, e.g. because of increasing interface scattering. We model this effect by using a first and second order correction term to model the changes of mobility as a function of V_{gsteff} so that this correction term can be included when the device is operated in the subthreshold region.

Methodology A: The parameter extraction is made difficult because two device parameters exist that have nearly identical effects on the on-state performance: the mobility degradation factor θ_1 and the device series resistance R_{SD}. Both effects are dependent on the applied V_{gs}. If the change in V_{gs} due to the voltage drop over the series source resistance is not taken into account, then they are interchangeable model parameters and related by $\theta_1 \Leftrightarrow \frac{W}{L}\mu_0 R_{SD}$.

One way to separate these two effects is to measure a series of devices with various channel lengths that are otherwise identical [26]. A linear extrapolation can be made to determine the series resistance of a “zero-length” device. This is problematic for the GAA InGaAs devices for two reasons: device variability and the influence of short channel effects.

The GAA InGaAs nanowire devices have significant variation in not only R_{SD}, but also other device parameters (e.g.

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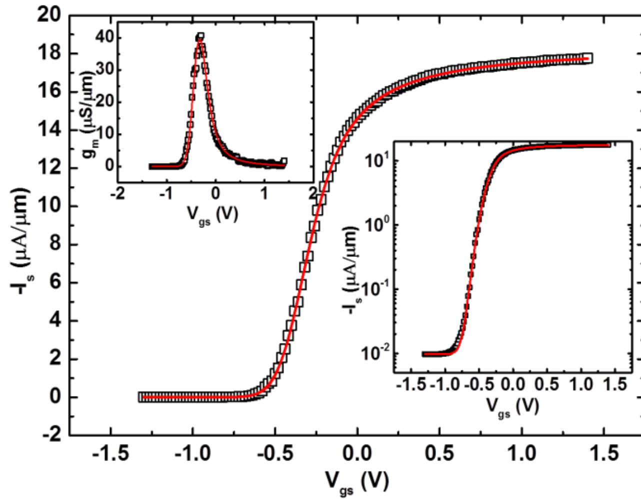

Fig. 10. Data from an array of four 30x30 nanowires measured at V_{ds}=50 mV, linear scale with an inlay of log scale I_s and linear scale g_m. Symbols are measured data points and lines are calculated based on the model parameters.

subthreshold slope and V_t, as seen in Fig. 13 and 14). These variations cause the extrapolation to be unreliable.

If short channel effects (e.g. threshold voltage shift and drain induced barrier lowering (DIBL)) are significant, then the relationship between the apparent R_{SD} (setting θ_1 to be zero) and the channel length will become non-linear, making it difficult to estimate the value at zero length.

Methodology B: An alternative method to determine R_{SD} is to perform $I_D - V_G$ measurements at multiple V_{DS} biases [27]. This method has the advantage that it only requires measurements from a single device, and as such, any variation between devices is irrelevant to the extraction. Also, it is resistant to short-channel effects because it only relies on low V_{ds} biases where short channel effects (if present) can be neglected.

As presented, this method compares the current at various V_{ds} biases at a fixed $(V_{gs} - V_t)$. Because of the low V_{ds} assumption and the equal gate biases, the mobility will be equal within each set of data. When using the square-law MOSFET model, the ratio of the currents can be analyzed, and gives a value that is independent of the mobility. The series resistance can be solved for in this case:

$$\frac{I_{D1}}{I_{D2}} = \frac{(V_{gs1} - V_{t1} - {I_{d1}R_{SD}}/{2})(V_{D1} - I_{D1}R_{SD})}{(V_{gs2} - V_{t2} - {I_{d2}R_{SD}}/{2})(V_{D2} - I_{D2}R_{SD})}$$

The threshold voltages can be extracted via the Y-function method [26], neglecting θ_2, by examining the Y-intercept of:

$$Y := \frac{I_D}{\sqrt{g_m}} \approx \sqrt{\mu_0 C_{ox} \frac{W}{L} V_{ds}(V_{gs} - V_t)}$$

By determining the value R_{SD} using this extraction method, and then fitting the measured data to the MOSFET model, the intrinsic device parameters can be determined. A non-linear solver is used to optimize the model parameters to best fit the measurement data.

As an example of this method, an array of four 30 nm by 30 nm nanowires with a gate length of 120 nm and an Al_2O_3 gate

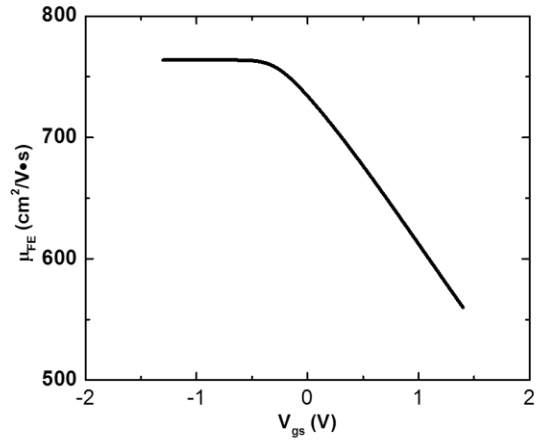

Fig. 11. Field effect mobility changes with V_{gs} in an array of four 30x30 NW devices.

dielectric with EOT=4.5 nm was measured. It was found to have a series resistance of 5503 Ω. The range in threshold voltage was -0.325 to -0.295 V from $V_{ds} = 5$ to 100 mV, respectively, confirming that short-channel effects are minimal and the low-V_{ds} assumption is valid. The mobility μ_0=764 cm^2/V s, while θ_1 is 0.11 /V. Similar to in Silicon NW devices [26], θ_2 is negligible, and is approximately 0.060 /V^2 for this InGaAs device. Output of these model parameters is shown in Fig. 10. The closeness of the modeled lines with the measured data for linear and log scale I_s, along with the transconductance g_m demonstrates the validity of the model. The mobility parameters θ_1, and θ_2 model how the mobility decreases as the gate voltage increases, as shown in Fig. 11. The mobility decreases to 713 cm^2/V s when I_s is 90% of its maximum (V_{gs}=0.3 V).

VI. Variability Induced Performance Drift

As the traditional devices scale down, the variability among transistors on a chip becomes prominent due to reasons such as random dopant fluctuation, random telegraphic noise, process variation, etc.[28-30] However, since the transistors based on nanowires typically have several NWs in parallel, there is an additional source of variability arising from the transport characteristics of different nanowires within a single transistor. As we will see, this sometimes leads to a systematic drift to the device performance as a function of the number of (parallel) nanowires within a given transistor. In this section, we will discuss how this NW-to-NW variability affects on-state and off-state parameters.

A. ON-state performance

We have seen in section III that how the on-current (I_{ON}) of a GAA MOSFET depends on channel length, nanowire dimension, and EOT. However, for a given set of such parameters, one would expect that I_{ON} should increase linearly with the number of parallel nanowires. For example, for a single nanowire transistor, the total on-current- $I_{ON,1} \sim V_{ds}/(R_{ch} + R_{SD})$, where V_{SD} is the drain voltage, R_{ch} is the channel resistance at the given condition, R_{SD} is the source-drain series resistance. For n number of nanowires in parallel, the expected

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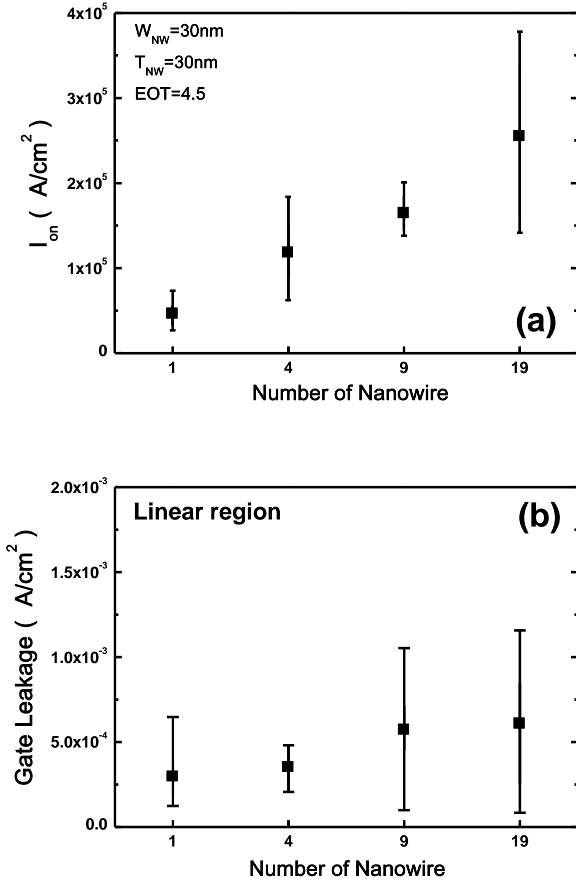

Fig. 12. (a) The on current density as a function of the number of parallel nanowires in a given transistor. Contrary to the planner devices, the current density increases with increasing the number of nanowires, or equivalently increasing the channel area. (b) The gate leakage density remains relatively unchanged with the number of nanowires, as expected, for the same set of devices.

total on-current is $I_{ON,n}{\sim}V_{ds}/(R_{ch}/n+R_{SD}/n)=n\times I_{ON,1}$, assuming that the total R_S is constant and consequently, the series resistance per nanowire is decreased with the increase of the number nanowires. Ideally, therefore, the *current density* (averaged over the total cross sectional area of all the nanowires) should remain constant regardless of the number of nanowires. Fig. 12(a) shows the average I_{ON} (A/cm^2) as a function of the number of nanowires in a given transistor. In this measurement, the width and thickness of each nanowire is 30nm, and EOT=4.5nm. Clearly, $I_{on}(\equiv I_{ON,n}/n)$ is not constant; rather, it increases as the number of nanowire increases! This implies that the series resistance per nanowire decreases super-linearly (i.e., smaller than R_{SD}/n) with the number of nanowires. Equivalently, the total R_S actually decreases with the increase of the nanowires. One might imagine the possibility of lesser current crowding for more number of nanowires leading to lower contact resistance [31]. However, further work is required for exact origin of such dependence of R_{SD} (and hence I_{ON}) on the number of nanowires.

For the same set of devices, the average gate leakage currents do not vary significantly with the number of nanowires (Fig. 12(b)), confirming that the nanowire dimensions are identical and the increase of I_{ON} in Fig. 12(a) cannot be attributed to process induced artifacts associated with increasing number of NW.

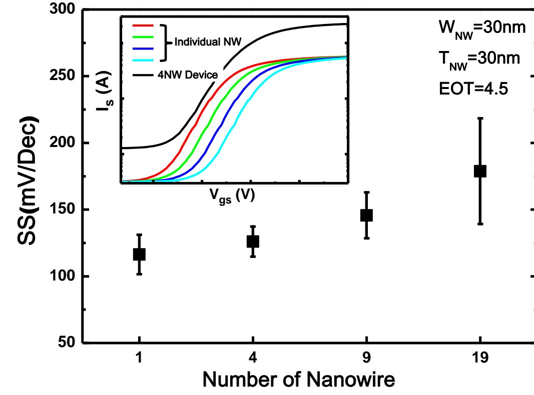

Fig. 13. SS as a function of the number of nanowires shows a performance degradation as the number of nanowire increases.

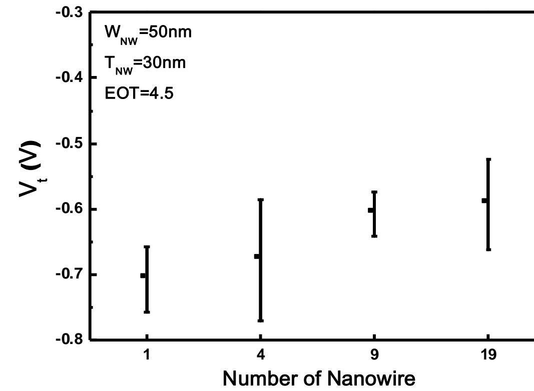

Fig. 14. V_t increases with the number of nanowire increases, possibly due to the self-heating effect and worse heat dissipation for higher number of parallel nanowires.

B. Off-State Performance

It has been discussed in section IV that the sub-threshold slope of the GAA InGaAs transistor could traditionally degrade due to short channel effect as well as the interface defects. Here we show another variability-induced SS degradation in the GAA transistors. Fig. 13 shows the SS measurements on the same set of devices as used in this section. The result shows more than 50% increase in SS as the number of nanowire increases from 1 to 19. This could be explained from the V_t variation within nanowires in a given transistor (Fig. 13 (inset)). With a given distribution of V_t, the nanowires start turning on sequentially as the voltage increases, giving rise to a higher SS.

Finally, Fig. 14 shows an increase of V_t as a function of the number of nanowires. The possible origin could lie on the self-heating effect, which increases the local temperature of the channel region during operation. Higher density of nanowires in a given transistor makes heat dissipation difficult, and the corresponding higher temperature may increase activated trapping of carriers within the gate oxides [32]. Such

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temperature-dependent trapping may increase V_t as a function of number of nanowires in a given transistor.

VII. Conclusion

InGaAs GAA nanowire MOSFETs offer a path towards the further scaling of transistors for ultimate CMOS technology development. They provide superior electrostatic control of the device channel, allowing higher on-current and lower SS and DIBL. We demonstrate various InGaAs nanowire MOSFETs using ALD gate dielectrics with EOT as low as 1.2 nm and electron mobility of 764 $cm^2/V\ s$ in the channel. Device performance and variability are examined experimentally with the trends associated with the device dimensions, EOT and interface quality.

Acknowledgement

The authors would like to thank M.S. Lundstrom, D.A. Antoniadis, J.A. del Alamo, Muhammad A. Wahab, Xinwei Wang, and Roy G. Gordon for valuable discussions and support in device fabrications.

References

[1] J. A. Del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature,* vol. 479, pp. 317-323, 2011.

[2] N. Goel, D. Heh, S. Koveshnikov, I. Ok, S. Oktyabrsky, V. Tokranov*, et al.*, "Addressing the gate stack challenge for high mobility In< inf> x</inf> Ga< inf> 1-x</inf> As channels for NFETs," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, 2008, pp. 1-4.

[3] J. Gu, A. Neal, and P. Ye, "Effects of (NH< inf> 4</inf>)< inf> 2</inf> S passivation on the off-state performance of 3-dimensional InGaAs metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters,* vol. 99, pp. 152113-152113-3, 2011.

[4] J. Gu, X. Wang, H. Wu, J. Shao, A. Neal, M. Manfra*, et al.*, "20-80nm Channel Length InGaAs Gate-all-around Nanowire MOSFETs with EOT= 1.2 nm and Lowest SS= 63mV/dec," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, p. 4.

[5] J. Huang, N. Goel, H. Zhao, C. Kang, K. Min, G. Bersuker*, et al.*, "InGaAs MOSFET performance and reliability improvement by simultaneous reduction of oxide and interface charge in ALD (La) AlOx/ZrO< inf> 2</inf> gate stack," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1-4.

[6] D.-H. Kim, P. Hundal, A. Papavasiliou, P. Chen, C. King, J. Paniagua*, et al.*, "E-mode planar L g= 35 nm In 0.7 Ga 0.3 As MOSFETs with InP/Al 2 O 3/HfO 2 (EOT= 0.8 nm) composite insulator," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, pp. 32.2. 1-32.2. 4.

[7] M. Si, J. J. Gu, X. Wang, J. Shao, X. Li, M. J. Manfra*, et al.*, "Effects of forming gas anneal on ultrathin InGaAs nanowire metal-oxide-semiconductor field-effect transistors," *Applied Physics Letters,* vol. 102, pp. 093505-093505-4, 2013.

[8] M. Yokoyama, T. Yasuda, H. Takagi, H. Yamada, N. Fukuhara, M. Hata*, et al.*, "Thin Body III--V-Semiconductor-on-Insulator Metal--Oxide--Semiconductor Field-Effect Transistors on Si Fabricated Using Direct Wafer Bonding," *Applied Physics Express,* vol. 2, p. 4501, 2009.

[9] H. Ko, K. Takei, R. Kapadia, S. Chuang, H. Fang, P. W. Leu*, et al.*, "Ultrathin compound semiconductor on insulator layers for high-performance nanoscale transistors," *Nature,* vol. 468, pp. 286-289, 2010.

[10] Y. Wu, R. Wang, T. Shen, J. Gu, and P. Ye, "First experimental demonstration of 100 nm inversion-mode InGaAs FinFET through damage-free sidewall etching," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1-4.

[11] H.-C. Chin, X. Gong, L. Wang, H. K. Lee, L. Shi, and Y.-C. Yeo, "III–V Multiple-Gate Field-Effect Transistors With High-Mobility," *Electron Device Letters, IEEE,* vol. 32, pp. 146-148, 2011.

[12] M. Radosavljevic, G. Dewey, J. Fastenau, J. Kavalieros, R. Kotlyar, B. Chu-Kung*, et al.*, "Non-planar, multi-gate InGaAs quantum well field effect transistors with high-k gate dielectric and ultra-scaled gate-to-drain/gate-to-source separation for low power logic applications," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, 2010, pp. 6.1. 1-6.1. 4.

[13] N. Singh, K. D. Buddharaju, S. Manhas, A. Agarwal, S. C. Rustagi, G. Lo*, et al.*, "Si, SiGe nanowire devices by top–down technology and their applications," *Electron Devices, IEEE Transactions on,* vol. 55, pp. 3107-3118, 2008.

[14] S. Bangsaruntip, G. Cohen, A. Majumdar, Y. Zhang, S. Engelmann, N. Fuller*, et al.*, "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1-4.

[15] P. Hashemi, L. Gomez, M. Canonico, and J. L. Hoyt, "Electron transport in gate-all-around uniaxial tensile strained-Si nanowire n-MOSFETs," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, 2008, pp. 1-4.

[16] J. Zhuge, R. Wang, R. Huang, Y. Tian, L. Zhang, D.-W. Kim*, et al.*, "Investigation of Low-Frequency Noise in Silicon Nanowire< emphasis emphasistype=," *Electron Device Letters, IEEE,* vol. 30, pp. 57-60, 2009.

[17] S. D. Suk, S.-Y. Lee, S.-M. Kim, E.-J. Yoon, M.-S. Kim, M. Li*, et al.*, "High performance 5nm radius Twin Silicon Nanowire MOSFET (TSNWFET): fabrication on bulk si wafer, characteristics, and reliability," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, 2005, pp. 717-720.

[18] J. Chen, T. Saraya, K. Miyaji, K. Shimizu, and T. Hiramoto, "Experimental study of mobility in [110]-and [100]-directed multiple silicon nanowire GAA MOSFETs on (100) SOI," in *VLSI Technology, 2008 Symposium on*, 2008, pp. 32-33.

[19] J. Gu, Y. Liu, Y. Wu, R. Colby, R. G. Gordon, and P. D. Ye, "First experimental demonstration of gate-all-around III–V MOSFETs by top-down approach," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, pp. 33.2. 1-33.2. 4.

[20] J. J. Gu, X. Wang, H. Wu, R. G. Gordon, and P. D. Ye, "Variability Improvement by Interface Passivation and EOT Scaling of InGaAs Nanowire MOSFETs," 2013.

[21] M. Lundstrom, "Elementary scattering theory of the Si MOSFET," *Electron Device Letters, IEEE,* vol. 18, pp. 361-363, 1997.

[22] A. Rahman, J. Guo, S. Datta, and M. S. Lundstrom, "Theory of ballistic nanotransistors," *Electron Devices, IEEE Transactions on,* vol. 50, pp. 1853-1864, 2003.

[23] J. J. Gu, H. Wu, Y. Liu, A. T. Neal, R. G. Gordon, and P. D. Ye, "Size-Dependent-Transport Study of< formula formulatype=," *Electron Device Letters, IEEE,* vol. 33, pp. 967-969, 2012.

[24] X. Sun and T. Ma, "Electrical Characterization of Gate Traps in FETs with Ge and III-V Channels," *Device and Materials Reliability, IEEE Transactions on,* vol. PP, pp. 1-1, 2013.

[25] X. J. Weidong Liu, J. Chen, M. Jeng, Z. Liu, Y. Cheng, K. Chen, M. Chan, K. Hui, J. Huang, R. Tu, P. Ko, and Chenming Hu. *BSIM3v2 MOSFET Model and Users' Manual*. Available: http://www-device.eecs.berkeley.edu/~bsim3

[26] K. Ye-Ram, L. Sang-Hyun, B. Chang-Ki, B. Rock-Hyun, Y. Kyoung-Hwan, K. Dong-Won*, et al.*, "Reliable extraction of series resistance in silicon nanowire FETs using Y-function technique," in *Nanotechnology Materials and Devices Conference (NMDC), 2011 IEEE*, 2011, pp. 262-265.

[27] J. P. Campbell, K. P. Cheung, L. C. Yu, J. S. Suehle, K. Sheng, and A. Oates, "New methods for the direct extraction of mobility and series resistance from a single ultra-scaled device," in *VLSI Technology (VLSIT), 2010 Symposium on*, 2010, pp. 75-76.

[28] K. K. Hung, P. K. Ko, H. Chenming, and C. Yiu Chung, "Random telegraph noise of deep-submicrometer MOSFETs," *Electron Device Letters, IEEE,* vol. 11, pp. 90-92, 1990.

[29] K. J. Kuhn, "Reducing Variation in Advanced Logic Technologies: Approaches to Process and Design for Manufacturability of Nanoscale CMOS," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 471-474.

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[30] X. Shiying and J. Bokor, "Sensitivity of double-gate and FinFETDevices to process variations," *Electron Devices, IEEE Transactions on,* vol. 50, pp. 2255-2261, 2003.

[31] N. K. S.-H. Park, D. Basu, Z. Jiang, S. K. Nayak, C. E. Weber, et al., "Scaling Effect on Specific Contact Resistivity in Nano-scale Metal-Semiconductor Contacts," presented at the Device Research Conference (DRC), Notre Dame, USA, 2013.

[32] H. Tien-Yu, C. Ting-Chang, C. Te-Chih, C. Yu-Te, T. Ming-Yen, C. Ann-Kuo*, et al.*, "Self-Heating-Effect-Induced Degradation Behaviors in a-InGaZnO Thin-Film Transistors," *Electron Device Letters, IEEE,* vol. 34, pp. 63-65, 2013.

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