Experimental Investigation of Border Trap Generation in InGaAs nMOSFETs With Al_2O_3 Gate Dielectric Under PBTI Stress

Guangfan Jiao, Chengjun Yao, Yi Xuan, *Member, IEEE*, Daming Huang, Peide D. Ye, and Ming-Fu Li

***Abstract*—The reliability performance of $In_xGa_{1-x}As$ n-type metal–oxide–semiconductor field-effect transistors with Al_2O_3 gate dielectric under positive-bias temperature instability stress is investigated systematically. A model of stress-induced border traps was proposed to interpret all charge pumping and I–V experimental results excellently. The stress-induced border traps include recoverable donor traps and permanent acceptor traps with respective energy densities $\Delta D_{\rm SOX}^{\rm Donor}(E)$ and $\Delta D_{\rm SOX}^{\rm Acceptor}(E)$. The shapes of $\Delta D_{\rm SOX}^{\rm Donor}(E)$ and $\Delta D_{\rm SOX}^{\rm Acceptor}(E)$ have been extracted from experimental data. $\Delta D_{\rm SOX}^{\rm Acceptor}(E)$ mainly distributes in the conduction band of InGaAs with a tail extending to the mid-gap, whereas $\Delta D_{\rm SOX}^{\rm Donor}(E)$ has a large distribution inside the energy gap and extends to the conduction band. The high density of $\Delta D_{\rm SOX}^{\rm Donor}(E)$ in the energy gap induces large degradation in the OFF-current, which is particularly serious when the In composition x is raised to 0.65.**

***Index Terms*—Border traps, InGaAs n-type metal–oxide–semiconductor field-effect transistors (nMOSFETs), OFF-current, positive-bias temperature instability (PBTI).**

I. Introduction

InGaAs has attracted much attention in the recent years as the channel material in n-type metal–oxide–semiconductor field-effect transistors (nMOSFETs) because of its higher electron mobility than that of silicon [1]–[7]. However, there are only a few studies reporting the reliability of InGaAs nMOSFETs [4], [6], [8]. We have investigated the reliability performance of InGaAs nMOSFETs under positive-bias temperature instability (PBTI) stress [9]. This paper elaborates more details than what was presented in [9].

II. Devices and Experiments

$In_xGa_{1-x}As$ nMOSFETs with $x = 0.53$ and 0.65 are used in this paper. The planar device structures and fabrication processes of these devices were illustrated in [3]. The transistors have channel width W of 100 μm, Al_2O_3 gate dielectric grown by Atomic Layer Deposition with physical thickness of 8 nm, and Ni/Au metal gate. P-type channel doping is about $1 - 2 \times 10^{17}$ cm^{-3}. Channel length L is 2–40 μm with specific value being marked in the relevant figure captions.

Current–voltage I–V and charge pumping (CP) measurements are carried out to characterize PBTI using an Agilent 4156C parameter analyzer, a pulse generator 81110A, and a Cascade probe station. In the I–V measurements, V_d is set to 50 mV, whereas the source and substrate are grounded ($V_s = V_b = 0$ V). In the conventional CP measurements [10], the source, drain, and substrate are all grounded. The CP current $I_{\rm cp}$ is measured from the source/drain. During the PBTI stress phase, the gate stress voltage $V_g = 3.0$ V, whereas $V_s = V_d = V_b = 0$ V. During the recovery phase, all the electrodes are grounded. All measurements are taken at room temperature. More than 20 devices for $x = 0.53$ and 0.65 nMOSFETs were measured, with the typical characteristics presented in this paper.

III. Experimental Results

A. CP Experiments

Fig. 1(a) shows the time evolution of the CP currents $I_{\rm cp}$ and the areal density of the stress-induced interface traps $\Delta N_{\rm it}$ for the $In_{0.65}Ga_{0.35}As$ nMOSFET during the PBTI stress phase and the following recovery phase. The interface trap density $N_{\rm it}$ is extracted from $I_{\rm cp}$ using the following formula [10]:

$$N_{\rm it} = I_{\rm cp}/(fqA_G) \tag{1}$$

where q is the proton charge, f is the pulse frequency, and A_G is the gate area. From the $I_{\rm cp}$ of the fresh device, the process-induced interface trap density $N_{\rm it}^0$ is derived to be about 9×10^{12} cm^{-2}. The stress-induced interface trap density $\Delta N_{\rm it} = N_{\rm it} - N_{\rm it}^0$ is only about 1.3×10^{11} cm^{-2} after 500-s stress. It decreases in the recovery phase. The inset in Fig. 1(a) illustrates that the time evolution of $\Delta N_{\rm it}$ in the stress phase shows a power law $\Delta N_{\rm it} \propto t^n$ with index $n = 0.22$, close to the index n of Si/SiON pMOSFET under negative bias temperature instability stress with similar CP measurement [11], [12].

Fig. 1(b) shows the frequency dependence of $N_{\rm it}^0$ and $\Delta N_{\rm it}$ estimated by CP experiments. By changing the CP frequency from 100 to 1 kHz, $N_{\rm it}^0$ increases by a factor of 1.3, whereas $\Delta N_{\rm it}$ increases by a factor of 2.5. The results indicate that the

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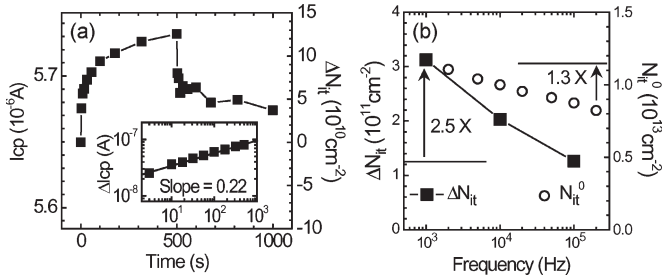

Fig. 1. (a) Time evolution of $I_{\rm cp}$ (left coordinate) and $\Delta N_{\rm it}$ (right coordinate) in stress phase (0–500 s) and recovery phase (500–1000 s). Channel $W/L = 100\ \mu{\rm m}/40\ \mu{\rm m}$. Inset: The time evolution of $\Delta I_{\rm cp}$ in the stress phase is plotted in log scale. (b) Frequency dependence of $N_{\rm it}^0$ (right coordinate) and $\Delta N_{\rm it}$ (left coordinate) estimated from CP experiments with the CP pulse rising and falling rates $dV/dt = 2\ {\rm V}/\mu{\rm s}$.

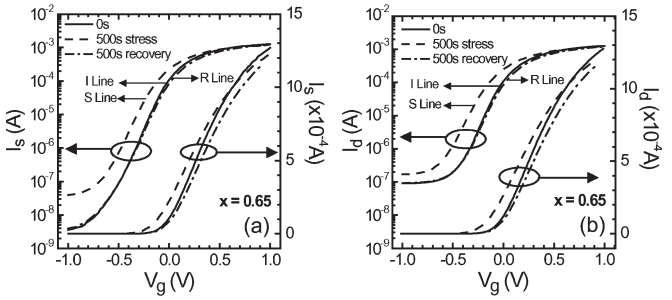

Fig. 2. (a) I_s–V_g and (b) I_d–V_g curves for the fresh $In_{0.65}Ga_{0.35}As$ nMOSFET (solid lines, denoted by I lines), after 500-s PBTI stress of $V_g = 3.0$ V (dashed lines, denoted by S lines), and after 500-s recovery of $V_g = 0$ V (dashed-dot lines, denoted by R lines). $V_d = 50$ mV in the I–V measurements. Channel $W/L = 100\ \mu{\rm m}/2\ \mu{\rm m}$.

stress-induced traps contain a major component of slow border traps (oxide traps near the interface) that can exchange electrons with the channel slowly. Therefore, the measured $\Delta N_{\rm it}$ has a strong CP frequency dependence, and the stress-induced traps are seriously underestimated by CP measurement [13]. We would thus denote the stress-induced traps by $\Delta N_{\rm SOX}$ rather than $\Delta N_{\rm it}$. Using the method illustrated in [13], the volume density of the stress-induced border traps can be estimated from Fig. 1(b) to be $\sim 5 \times 10^{18}\ {\rm cm}^{-3}$.

B. I_s–V_g Experiments

Fig. 2 shows the I_s–V_g and I_d–V_g characteristics measured from devices with $x = 0.65$ before stress (initial state, I lines), after 500-s PBTI stress (S lines), and with additional 500-s recovery (R lines). Both I_s–V_g and I_d–V_g show the same characteristics except in the "OFF-current" region. In this region, I_d is larger than I_s and is confirmed to be the drain leakage flowing to the substrate when a V_d of 50 mV is applied. This leakage is further discussed in Section V. In the following investigation, we will mainly use I_s–V_g as the transfer characteristic.

Fig. 3 shows the I_s–V_g characteristics measured before stress (initial state, I lines), after 500-s PBTI stress (S lines), and with additional 500-s recovery (R lines) for $x = 0.65$ and 0.53 devices. There are two points worth to be noticed. First, by comparing the I and S lines, ΔV_g extracted at low I_s [subthreshold (SS) region] is negative after stress, accompanied by a degradation in SS swing S, as shown in Figs. 3–5(a).

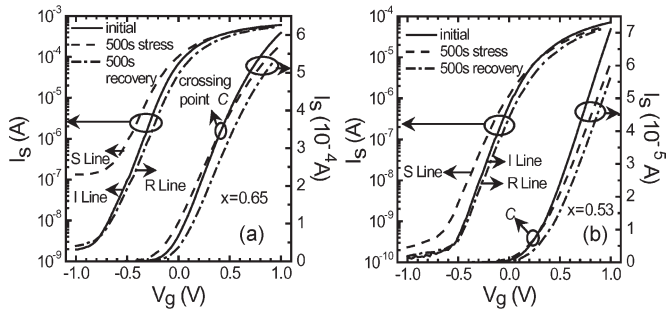

Fig. 3. I_s–V_g curves for the fresh $In_xGa_{1-x}As$ nMOSFET (solid lines, denoted by I lines), after 500-s PBTI stress (0–500 s, $V_g = 3.0$ V) (dashed lines, denoted by S lines), and then after 500-s recovery (500–1000 s, $V_g = 0$ V) (dashed-dot lines, denoted by R lines). $V_d = 50$ mV. (a) $x = 0.65$, $W/L = 100\ \mu{\rm m}/4\ \mu{\rm m}$. (b) $x = 0.53$, $W/L = 100\ \mu{\rm m}/8\ \mu{\rm m}$. Comparing S lines with R lines, the V_g shift ΔV_g at constant current I_s is negative in the SS region, accompanied by the degradation in S, supporting the donor trap [7] generation under stress. ΔV_g is positive at high I_s in the ON-current region due to the acceptor traps generation, accompanied by the degradation in G_m. A crossing point C is defined at $\Delta V_g = 0$.

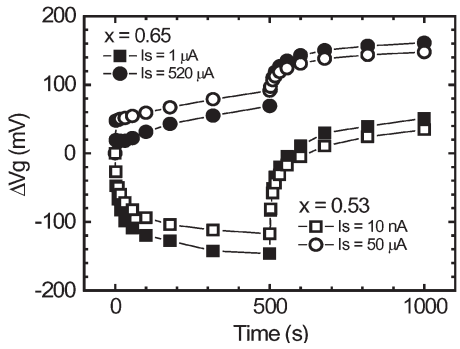

Fig. 4. Time evolution of ΔV_g in the SS region and in the ON-current region in stress and recovery phase. The results are extracted from $x = 0.53$ and 0.65 devices. ΔV_g in the ON-current region continuously increases in the recovery phase. ΔV_g in the SS region turns to positive at the end of the recovery phase.

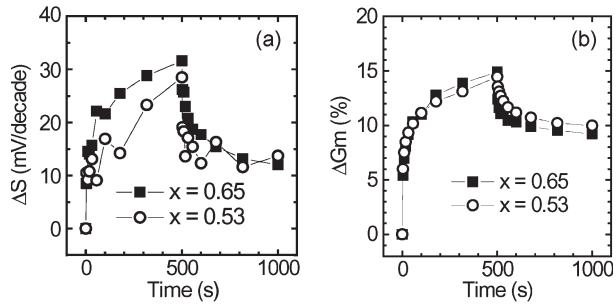

Fig. 5. Time evolution of (a) the ΔS extracted at $I_s = 5.0\ \mu$A for $x = 0.65$ device and that extracted at $I_s = 10$ nA for $x = 0.53$ device. (b) Time evolution of the degradation in transconductance extracted from $x = 0.53$ and 0.65 devices.

ΔV_g extracted at high I_s ("ON-current" region) is positive after stress, accompanied by a degradation in transconductance G_m, as shown in Figs. 3–5(b). There is a crossing point between the I and S lines, denoted by C, at which $\Delta V_g = 0$. Second, by comparing the I and R lines, ΔV_g extracted at low I_s in the SS region is positive, with a degradation in S, as shown in Figs. 3–5(a). The strange thing is that, at high I_s, ΔV_g increases

further in the recovery phase, as shown in Figs. 3 and 4, and it saturates gradually toward a constant value.

IV. Border Trap Model

At first glance at the I_s–V_g curves in Fig. 3, one may consider the stress-induced donor traps to be responsible for the negative ΔV_g and the degradation in S in the SS region [comparing the I and S lines in Figs. 3 and 11(a) in [7]]. One may also consider the stress-induced acceptor traps or the fixed charge to be responsible for the positive ΔV_g in the high I_s region and the degradation in transconductance G_m, as shown in Figs. 3–5(b). However, there are several conflicting points that have to be considered in the analyses presented in [9]. The key point is that the stress-induced donor traps estimated from ΔV_g shown in Fig. 3 are in the range of 10^{12} cm^{-2} (see Section VI), which is one order of magnitude higher than that estimated from the CP measurement shown in Fig. 1(a). Combining with the results shown in Fig. 1(b), it is obvious that the stress-induced traps are mainly not the conventional interface traps, but the border traps near the interface in the oxide layer. The electron capture by or emission from the border traps cannot follow the fast change of the surface potential in the CP measurement. As a result, $\Delta N_{\rm SOX}$ is seriously underestimated by the CP measurement [13]. However, electron trapping (detrapping) can follow the slow change of the surface potential in the I_s–V_g measurement and cause the change in V_g and the degradation in S in the SS region, acting as a role similar to conventional interface traps [14].

We now compare the R lines with I lines in Fig. 3 in the SS region. There are two possible cases to be considered after the recovery phase. 1) There are recoverable donor traps and permanent acceptor traps, which can explain the positive ΔV_g and the S degradation [see the difference between the I and R lines and compare it with Fig. 11(b) in [7]]. 2) There are recoverable donor traps and fixed negative oxide charge. In the case 2, the R lines in Fig. 3 are the combined effect of the fixed charge and the residual donor traps. The fixed charge induces a parallel positive shift in the I_s–V_g curve. The residual donor traps induce the degradation in S and the negative ΔV_g. If it is case 2, the residual donor traps must have high enough density to compensate the positive shift induced by the fixed charge. As a result, the net ΔV_g is close to zero only when I_s is very low (4×10^{-9} A for $x = 0.65$ devices and 3×10^{-10} A for $x = 0.53$ devices), as shown in Fig. 3. Case 2 should be ruled out because the recovered OFF-current $I_s^{\rm off}$ (discussed in Section V) reveals that the stress-induced donor traps mostly recovered in the end of the recovery phase. These results are in conflict with case 2, but in support of case 1.

A unified and natural border trap model has emerged to explain perfectly all the details of the aforementioned experimental results, as shown in Fig. 6. The main points of this model are as follows:

1) The stress-induced slow border traps with density $\Delta D_{\rm SOX}$ include recoverable donor traps with energy density $\Delta D_{\rm SOX}^{\rm Donor}(E)$ and permanent acceptor traps with energy density $\Delta D_{\rm SOX}^{\rm Acceptor}(E)$.

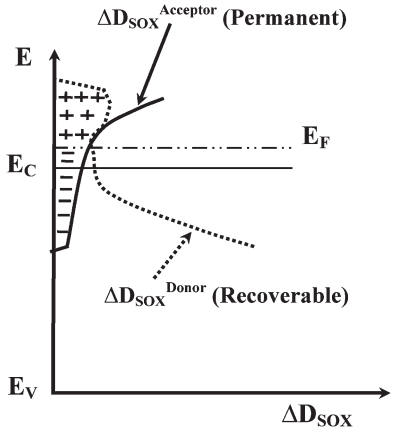

Fig. 6. Stress-induced trap density $\Delta D_{\rm SOX}(E)$ that consists of permanent acceptor traps $\Delta D_{\rm SOX}^{\rm Acceptor}$ (solid line) and recoverable donor traps $\Delta D_{\rm SOX}^{\rm Donor}$ (dashed line). During the I_s–V_g measurement, when E_F is moved to a level above E_C, the positive charge in the donor traps is equal to the negative charge in the acceptor traps, corresponding to the crossing point C at which $\Delta V_g = 0$ in Fig. 3.

2) The recoverable $\Delta D_{\rm SOX}^{\rm Donor}(E)$ not only distributes within the InGaAs energy gap but also extends to the conduction band. The donor traps within the energy gap induce the negative ΔV_g and the S degradation in the stress phase and the recovery in the SS region during the recovery phase [Figs. 3–5(a)]. The donor traps in the conduction band induce the strange phenomena of continuous increase of positive ΔV_g in the recovery phase (Figs. 3 and 4).
3) The permanent $\Delta D_{\rm SOX}^{\rm Acceptor}(E)$ mainly distributes in the conduction band with a tail extending to the energy gap. The acceptor traps in the conduction band induce the positive ΔV_g and the degradation in G_m in the high I_s region in the stress phase [Figs. 3–5(b)]. The acceptor traps in the energy gap result in the positive ΔV_g and the small S degradation in the SS region at the end of the recovery phase [Figs. 3–5(a)].
4) All the border traps are seriously underestimated by the CP measurements when they cannot follow the fast change of the surface potential during the CP measurements.

V. OFF-Current Degradation

In this section, we concentrate on the degradation behavior of the OFF-current in the range of $V_g = -0.8$ to -1.0 V, denoted by $I_s^{\rm off}$. As shown in Fig. 3, for $V_g = -0.8$ to -1.0 V, $I_s^{\rm off}$ is nearly independent of V_g. Fig. 7 shows the time evolutions of the $I_s^{\rm off}$ change ($\Delta I_s^{\rm off}$) at a constant gate voltage $V_g = -0.8$ V in the stress and recovery phases for $x = 0.65$ and 0.53 devices, respectively. As shown, $\Delta I_s^{\rm off}$ increases with time in the stress phase and almost completely recovers in the recovery phase, implying that $\Delta I_s^{\rm off}$ is related to the generation of recoverable donor traps, as discussed in Section IV. However, as shown in Fig. 3, both $I_s^{\rm off}$ and $\Delta I_s^{\rm off}$ show a large quantitative difference between $x = 0.53$ and 0.65 devices. For $x = 0.53$ devices, the $I_s^{\rm off}$ is in the range of 10^{-10} A in the initial state. It increases by a factor of 2–3 after 500-s stress. For $x = 0.65$ devices,

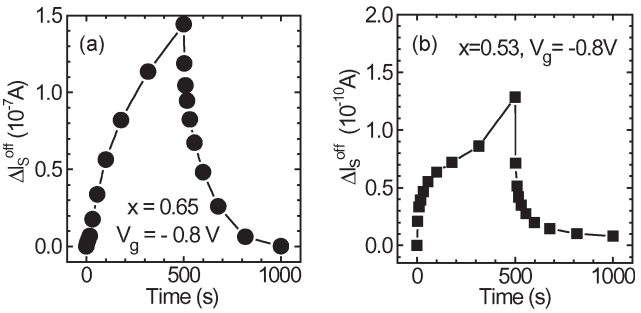

Fig. 7. Time evolutions of $\Delta I_s^{\rm off}$ at constant gate voltage $V_g = -0.8$ V in the stress and recovery phases for (a) $x = 0.65$ and (b) $x = 0.53$ devices.

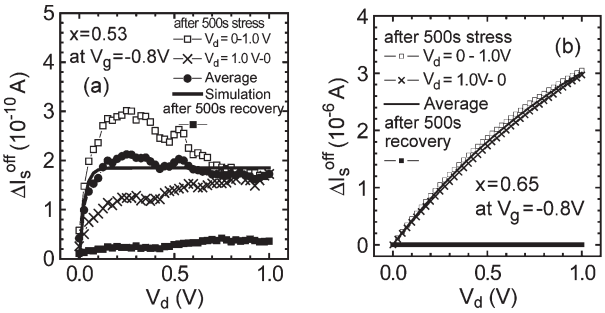

Fig. 8. (a) $\Delta I_s^{\rm off} - V_d$ curves after 500-s PBTI stress and after 500-s recovery for the $x = 0.53$ nMOSFET. The measured $\Delta I_s^{\rm off} - V_d$ is distorted by the recovery effect during the measurement. To avoid this distortion, we first scan V_d from 0 to 1.0 V (symbol □). The distortion (reduction of $\Delta I_s^{\rm off}$) is larger when V_d is higher due to a longer measurement time. We then scan from 1.0 to 0 V (symbol ×). The distortion in this case is larger when V_d is smaller. The average of two curves (symbol •) approximately gives the undistorted $\Delta I_s^{\rm off} - V_d$ measured during the time of V_d scanning. The result is in well agreement with the theoretical prediction by (2) (solid curve). (b) The same as (a) but for $x = 0.65$ nMOSFET, showing that $\Delta I_s^{\rm off} - V_d$ after 500-s PBTI stress does not satisfy (2).

however, the $I_s^{\rm off}$ is in the range of 10^{-9} A in the initial state. It increases by two orders of magnitude after 500-s stress.

Fig. 8 illustrates the $\Delta I_s^{\rm off} - V_d$ curves measured after 500-s stress and 500-s recovery for $x = 0.53$ and 0.65 devices. If $\Delta I_s^{\rm off}$ is due to the change of the surface potential pinning [8], [15], $\Delta I_s^{\rm off}$ should be the diffusion current of minority carriers in the SS region and should satisfy the following equation [14]:

$$\Delta I_s^{\rm off} = A\,[1 - \exp(-qV_d/kT)] \tag{2}$$

which saturates when $V_d > 3$ kT/q ≈ 0.1 V. As shown in Fig. 8(a), for $x = 0.53$ devices with $I_s^{\rm off}$ in the range of 10^{-10} A, $\Delta I_s^{\rm off}$ measured after 500-s stress satisfies (2). The results imply that the degradation (recovery) of $\Delta I_s^{\rm off}$ is due to the generation (recovery) of a large density of donor traps in the energy gap, causing the change of the surface potential pinning. However, as shown in Fig. 8(b) for $x = 0.65$ devices with $I_s^{\rm off}$ in the range of $10^{-9} - 10^{-7}$ A, $\Delta I_s^{\rm off}$ measured after 500-s stress does not satisfy (2). In that case, $\Delta I_s^{\rm off}$ is likely due to the drift of electrons in a surface conduction path across the source and drain, and therefore, the $I_s^{\rm off}$–V_d relationship is similar to the case of an ohmic resistance. Fig. 9 shows the I_d and I_s versus V_d curves ($V_g = -0.8$ V) for the initial state, after 500-s stress, and after 500-s recovery for $x = 0.53$ and 0.65 devices. The I_d in the both kinds of devices are pretty

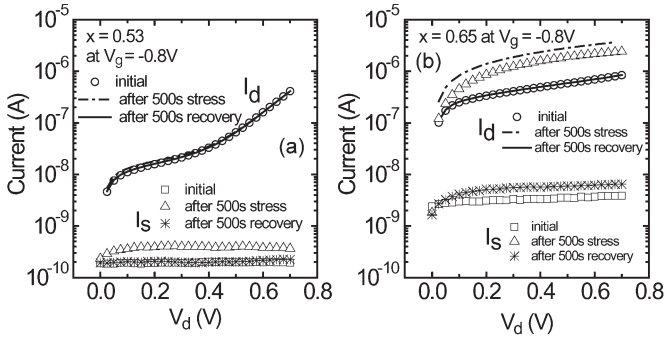

Fig. 9. I_d and I_s versus V_d at $V_g = -0.8$ V for (a) $x = 0.53$ and (b) $x = 0.65$ nMOSFETs in the initial state, after 500-s PBTI stress, and after 500-s recovery. The substrate current $I_{\rm sub}$ is also measured, which satisfies $I_{\rm sub} = I_d - I_s$. For the $x = 0.65$ device, there is a large component (10^{-6} A) of stress induced I_s flowing from the drain.

large ($> 10^{-7}$ A) when $V_d > 0.8$ V. A major component of the I_d is the pn-junction reverse bias leakage I_{jl}. In this paper, the transistor channel length L_g is near 4–8 μm, with a similar drain size L_d along the channel direction. Since $I_{\rm on}$ and I_{jl} are proportional to L_g^{-1} and L_d, respectively, when L_g and L_d are reduced to the nanometer range, $I_{\rm on}/I_{jl}$ can be improved by several orders of magnitude. I_{jl} can be further improved by reducing s/d activation temperature [3] or by using an implant-free 3-D structure [16]. Figs. 8(b) and 9(b) show that for the $x = 0.65$ devices, about one-half of the stress-induced drain current flows to the source through a channel surface conduction path. This surface conduction path could be due to the hopping conduction [17] between the neighboring donor traps induced by the stress. Although a high In mole fraction x can improve the ON-current performance of $In_xGa_{1-x}As$ nMOSFETs, the large $\Delta I_s^{\rm off}$ in $x = 0.65$ devices raises a new challenge for developing III–V MOSFET technology for low standby power application. Further improvement in high-k/InGaAs interface quality, in particular, reducing the interface trap and border trap densities within the lower half energy gap, is needed to suppress the OFF-current degradation of InGaAs MOSFETs. New passivation techniques and alternative high-k dielectrics are being explored.

VI. Extractions of Border Trap Densities From Experiments

We can use the I_s–V_g curves in Fig. 3 to estimate the energy distribution of stress-induced border traps based on the following assumptions for the trap model described in Section V. 1) At the end of 500-s stress, there are both stress-induced donor traps and acceptor traps in the devices. 2) At the end of 500-s recovery, the stress-induced donor traps fully recover while the acceptor traps are permanent.

A. Method I—Extraction From ΔV_g in the I_s–V_g Curves

At first, ΔV_g is extracted from the I and R lines as a function of I_s for all the current ranges shown in Fig. 3. The result is denoted by $\Delta V_g^{\rm IR}(I_s)$. Since only the acceptor traps remain after 500-s recovery, the density $\Delta N_{\rm SOX}^{-\ {\rm Acceptor}}(I_s)$ of

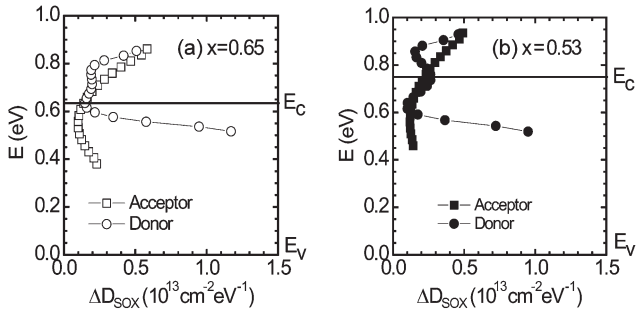

Fig. 10. Donor and acceptor trap energy densities extracted from (6) and (7) for (a) $In_{0.65}Ga_{0.35}As$ and (b) $In_{0.53}Ga_{0.47}As$ nMOSFETs.

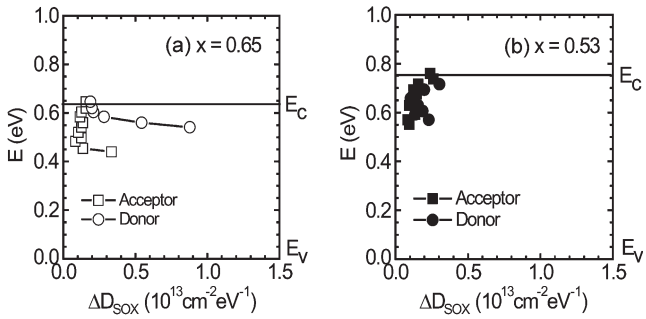

Fig. 11. Donor and acceptor trap energy densities extracted from (8) and (10) for (a) $In_{0.65}Ga_{0.35}As$ and (b) $In_{0.53}Ga_{0.47}As$ nMOSFETs.

negatively charged acceptor traps as a function of I_s can be obtained by

$$\Delta N_{\rm SOX}^{-\ \rm Acceptor}(I_s) = (C_{\rm OX}/q)\Delta V_g^{\rm IR}(I_s) \tag{3}$$

where $C_{\rm OX}$ is the gate oxide capacitance per unit area and is near 10^{-6} F/cm^2 estimated using 8-nm Al_2O_3 gate dielectric. The density difference of negatively charged acceptor traps and positively charged donor traps $\Delta N_{\rm SOX}^{-\ \rm Acceptor}(I_s) - \Delta N_{\rm SOX}^{+\ \rm Donor}(I_s)$ can be extracted from the I and S lines, shown in Fig. 3, by

$$\Delta N_{\rm SOX}^{-\ \rm Acceptor}(I_s) - \Delta N_{\rm SOX}^{+\ \rm Donor}(I_s) = (C_{\rm OX}/q)\Delta V_g^{\rm IS}(I_s) \tag{4}$$

where $\Delta V_g^{\rm IS}(I_s)$ is the V_g difference between the S and I lines at the same I_s. From (3) and (4), the density of positively charged donor traps can be obtained from

$$\Delta N_{\rm SOX}^{+\ \rm Donor}(I_s) = (C_{\rm OX}/q)\Delta V_g^{\rm IR}(I_s) - (C_{\rm OX}/q)\Delta V_g^{\rm IS}(I_s). \tag{5}$$

Next, the surface potential ψ_s and the energy difference $E = E_F - E_V$ at the interface as a function of I_s can be calculated by SILVACO Atlas simulation tool for $In_xGa_{1-x}As$ nMOSFETs. The device structures for simulation are the same as the real devices reported in [3]. From these simulations, the relationship between I_s and the energy $E(I_s)$ is obtained. Combining (3), (5), and $E(I_s)$, we obtain $\Delta N_{\rm SOX}^{+\ \rm Donor}(E)$ and $\Delta N_{\rm SOX}^{-\ \rm Acceptor}(E)$ as functions of E. The energy distribution of donor and acceptor traps can be obtained from

$$\Delta D_{\rm SOX}{}^{\rm Donor}(E) = -\frac{d\Delta N_{\rm SOX}^{+\ \rm Donor}}{dE} \tag{6}$$

$$\Delta D_{\rm SOX}{}^{\rm Acceptor}(E) = \frac{d\Delta N_{\rm SOX}^{-\ \rm Acceptor}}{dE}. \tag{7}$$

The results are plotted in Fig. 10.

There are two possible error sources in obtaining the donor and acceptor trap densities using the above derivations. 1) The mobility degradation induced ΔV_g in the strong inversion region has been overlooked [18]. Therefore, both donor and acceptor trap densities may be overestimated, giving rise to the distortions of the curves in the horizontal direction in Fig. 10 in the conduction band region. 2) The Atlas simulator for III–V MOSFET simulation is not matured and may introduce some error in $E(I_s)$ relation, giving rise to the distortions of the curves in the vertical direction in Fig. 10. In spite of these distortions, the overall energy distributions of donor and acceptor traps demonstrated in Fig. 10 can excellently explain all the experimental results. The stress-induced donor traps have a large density in the energy gap, and their distribution extends to the conduction band. These traps are almost completely recovered when the stress is terminated. The stress-induced permanent acceptor traps are mainly distributed in the conduction band, with a tail extending to the mid-gap.

B. Method II—Extraction From the Degradation in S in the SS Region

We can also extract part of the energy distribution of stress-induced traps from the ΔS in the SS region. On the one hand, since only the acceptor traps remain after 500-s recovery, their energy distribution $\Delta D_{\rm SOX}^{\rm Acceptor}(I_s)$ can be obtained from [14]

$$\Delta D_{\rm SOX}^{\rm Acceptor}(I_s) = [C_{\rm OX}/(qkTln10)]\,\Delta S^{\rm IR}(I_s) \tag{8}$$

where $\Delta S^{\rm IR}(I_s)$ is the difference in S extracted between the R and I lines shown in Fig. 3, k is Boltzmann's constant, and T is the absolute temperature. On the other hand, the sum of the acceptor and donor traps $\Delta D_{\rm SOX}^{\rm Acceptor}(I_s) + \Delta D_{\rm SOX}^{\rm Donor}(I_s)$ can be extracted from the I and S lines using

$$\Delta D_{\rm SOX}^{\rm Acceptor}(I_s) + \Delta D_{\rm SOX}^{\rm Donor}(I_s) = [C_{\rm OX}/(qkTln10)]\,\Delta S^{\rm IS}(I_s) \tag{9}$$

where $\Delta S^{\rm IS}(I_s)$ is the difference in S extracted between the I and S lines, as shown in Fig. 3. From (8) and (9), the energy distribution of donor traps $\Delta D_{\rm SOX}^{\rm Donor}(I_s)$ can be obtained from

$$\Delta D_{\rm SOX}^{\rm Donor}(I_s) = [C_{\rm OX}/(qkTln10)]\,\Delta S^{\rm IS}(I_s) - [C_{\rm OX}/(qkTln10)]\,\Delta S^{\rm IR}(I_s). \tag{10}$$

By combining (8), (10), and the simulation result $E(I_s)$ described in Method I, we obtain $\Delta D_{\rm SOX}^{\rm Donor}$ and $\Delta D_{\rm SOX}^{\rm Acceptor}$ as functions of energy E. The results shown in Fig. 11 are only in a narrow energy region corresponding to the SS region in the I_s–V_g curves. However, the trap energy distributions estimated from Methods I and II are consistent in the same energy range.

VII. Conclusion

We have presented CP and I_s–V_g degradations under PBTI stress for $In_xGa_{1-x}As$ nMOSFETs with $x = 0.53$ and 0.65. A model for the slow border traps induced by stress near the Al_2O_3/InGaAs interface is proposed to perfectly interpret all experimental results in detail. The stress-induced border traps include recoverable donor traps with energy density $\Delta D_{\rm SOX}^{\rm Donor}(E)$ and permanent acceptor traps with energy density $\Delta D_{\rm SOX}^{\rm Acceptor}(E)$, which can be estimated from the measured I_s–V_g curves. The permanent $\Delta D_{\rm SOX}^{\rm Acceptor}(E)$ distributes mainly in the conduction band of InGaAs with a tail extending to the mid-gap. It is responsible for the positive ΔV_g in the ON-current region of the I_s–V_g curve after stress. The recoverable $\Delta D_{\rm SOX}^{\rm Donor}(E)$ has a large distribution in the InGaAs energy gap and extends to the conduction band. It is responsible for the negative ΔV_g in the SS region, the S degradation, the $I_s^{\rm off}$ degradation of the I_s–V_g curve in the stress phase, and continuous degradation of positive ΔV_g in the ON-current region in the recovery phase. The $\Delta D_{\rm SOX}^{\rm Donor}(E)$ is completely recoverable in the recovery phase. The large $I_s^{\rm off}$ degradation under stress for $In_{0.65}Ga_{0.35}As$ nMOSFETs exposes new challenges in the technology development of InGaAs nMOSFET.

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