0.1-μm InAlN/GaN High Electron-Mobility Transistors for Power Amplifiers Operating at 71–76 and 81–86 GHz: Impact of Passivation and Gate Recess

Dong Xu, *Senior Member, IEEE*, Kanin Chu, Jose A. Diaz, Michael D. Ashman, J. J. Komiak, *Fellow, IEEE*, Louis M. Mt. Pleasant, Alice Vera, Philip Seekell, Xiaoping Yang, Carlton Creamer, K. B. Nichols, K. H. George Duh, *Senior Member, IEEE*, Phillip M. Smith, *Fellow, IEEE*, P. C. Chao, *Fellow, IEEE*, Lin Dong, and Peide D. Ye, *Fellow, IEEE*

***Abstract*— We have developed 0.1-μm gate-length InAlN/GaN high electron-mobility transistors (HEMTs) for millimeter-wave (MMW) power applications, particularly at 71–76 and 81–86 GHz bands. The impacts of depth and width of the gate recess groove on electrical performance have been analyzed and compared. Competing passivation technologies, atomic layer deposition (ALD) aluminum oxide (Al_2O_3) and plasma-enhanced chemical vapor deposition (PECVD) SiN, have also been assessed in terms of dc, pulsed-IV, and high-frequency characteristics. It has been found that while PECVD SiN-passivated HEMTs and the monolithic microwave integrated circuits slightly underperform their ALD Al_2O_3-passivated counterparts, their MMW power performance can be further boosted with the gate recess due to the improved aspect ratio and scaling characteristics. When biased at a drain voltage of 10 V, a first-pass two-stage power amplifier design based on recessed PECVD SiN-passivated 0.1-μm depletion-mode devices has demonstrated an output power of 1.63 W with a 15% power-added efficiency at 86 GHz.**

***Index Terms*— Aluminum oxide (Al_2O_3), atomic layer deposition (ALD), GaN, high electron-mobility transistor (HEMT), InAlN, millimeter-wave (MMW) power amplifier (PA), passivation.**

I. Introduction

IN THE pursuit of devices for power amplifiers (PAs) operating at 71 GHz and beyond, there have already been a few pieces of noteworthy work reported in the past several years, with the best AlGaN/GaN high electron-mobility transistor (HEMT) based monolithic microwave integrated circuits (MMICs) demonstrating an output power (P_{out}) of 1–2 W and a power added efficiency (PAE) of 6%–19% in the frequency range of 76–96 GHz [1]–[4]. As a new contender for next-generation millimeter-wave (MMW) PAs, the HEMT based on InAlN/GaN heterojunction, lattice matched to SiC substrate, has recently generated a lot of interest. This is largely due to its high sheet carrier density that would allow more aggressive gate-length scaling without excessive compromise in aspect ratio, excellent thermal stability as reported in [5] and [6], and the resulting potential reliability advantage as well. Some encouraging progress has been made; for instance, InAlN/GaN HEMTs have shown good power performance at 30–40 GHz [7]–[9]. The key to achieving excellent power performance in the MMW range is to address the conflict between the thinner gate layer required by the short gate length needed for high-frequency operation and the increasingly adverse impact of surface traps on the current-carrying channel layer. Apparently, the most straightforward strategy is to protect the surface of the InAlN/GaN HEMT properly so that trapping effects would be less pronounced [10]–[12] or to keep the channel sufficiently away from the surface to minimize the impact.

In this paper, we will report the short gate-length InAlN/GaN HEMTs developed for PAs targeting E-band (71–76 and 81–86 GHz) applications. A gate length of 0.1 μm has been selected to meet the requirement of high operating frequency while keeping short channel effects to a minimum. Atomic layer deposition (ALD) aluminum oxide (Al_2O_3) and plasma-enhanced chemical vapor deposition (PECVD) SiN have been evaluated and compared as competing passivation technologies. Meanwhile, the use of a gate recess process has also been investigated as an important technical solution to improving the power performance of InAlN/GaN HEMTs. This is because gate recess etching would allow the adoption of a thicker top barrier for devices while still maintaining an excellent aspect ratio by placing the gate electrode sufficiently close to the channel.

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L. Dong was with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA. He is now with Applied Materials, Inc., Santa Clara, CA 94085 USA (e-mail: Lin_Dong@amat.com).

P. D. Ye is with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA (e-mail: yep@purdue.edu).

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II. Fabrication Technology

The 0.1-μm InAlN/GaN HEMTs were fabricated based on the InAlN/GaN heterostructure grown by metalorganic chemical vapor deposition on 4-in semi-insulating SiC substrates. The epitaxial structure includes a thin AlN nucleation layer, an undoped AlGaN buffer, an undoped GaN channel layer less than 100 nm, a nominally 1-nm undoped AlN layer, and a nominally 5-nm undoped InAlN gate layer with 17% indium. The device has a source–drain spacing of 2 μm, and the 0.1-μm Γ-gate is placed at about 0.5 μm from the source. For recessed devices, BCl_3 plasma was used to remove about 3-nm recess InAlN barrier layer before the gate metallization, thus reducing the gate-to-channel distance to 3 from 6 nm. More details on the fabrication process can be found in [13]. To further enhance the MMW performance, the SiC substrate is thinned down to 2 mil, enabling the fabrication of 15 μm $\times$ 25 μm slot via holes for realizing low inductance and more compact devices to facilitate MMW MMIC design [14].

Three wafers have been included for this paper: Wafer A was passivated with ALD Al_2O_3 as described in [15], while Wafers B and C were passivated with PECVD SiN. The thicknesses of dielectric passivation films for Wafers A and B differ by approximately 5%; the passivation layer on Wafer C is approximately 30% thinner than Wafer B. The total thicknesses of passivation layers are below 100 nm for all the three wafers in order to extract more gain from devices for operation at E-band. Meanwhile, for each of the three wafers, two types of devices were fabricated:

1) the unrecessed, whose epitaxial layer was not recess etched before the gate metal deposition;
2) the recessed, which was etched both vertically ($\sim$3 nm) and laterally using BCl_3 plasma before the gate metallization onto the InAlN layer.

While the lateral recess widths are comparable to the gate length of devices for all the three wafers, Wafer A has the widest recess groove; in comparison, the recess widths of Wafers B and C are about 20% and 30% smaller, respectively.

Also included in the discussion is a special type of device, which was recessed only vertically under the gate without a lateral etching. This is to facilitate the analysis of the individual impact of vertical and lateral recess on the electrical performance of the devices.

III. Device Results and Discussion

A. Output and Transfer Characteristics

Generally speaking, the passivation technique does not result in an apparent difference in dc characteristics. Fig. 1(a) and (b) is the IV and transfer characteristics of the Al_2O_3-passivated (Wafer A, dotted lines) and SiN-passivated HEMTs (Wafers B and C, plotted with solid and dashed lines, respectively) without gate recess. The Al_2O_3-passivated device shows a maximum drain current (I_{max}) of about 1.8 A/mm at a gate bias V_{gs} of 1 V and a drain bias V_{ds} of 10 V, a few percentage points higher than those of the SiN-passivated devices. In addition to the same sharp pinchoff characteristics, similar maximum extrinsic transconductances (g_{max}) as high as 770, 745, and 755

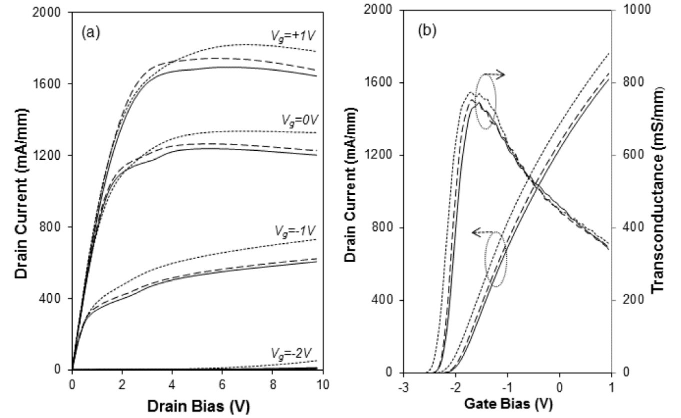

Fig. 1. (a) Output IV characteristics and (b) transfer curves and transconductance for unrecessed 0.1-μm InAlN/GaN HEMTs fabricated on Wafers A (dotted lines), B (solid lines), and C (dashed lines). The gate bias for the top curve of the IV characteristics is 1 V and the step of the gate bias is -1 V for all the three devices. The transfer curves and transconductances were measured at a V_{ds} of 10 V.

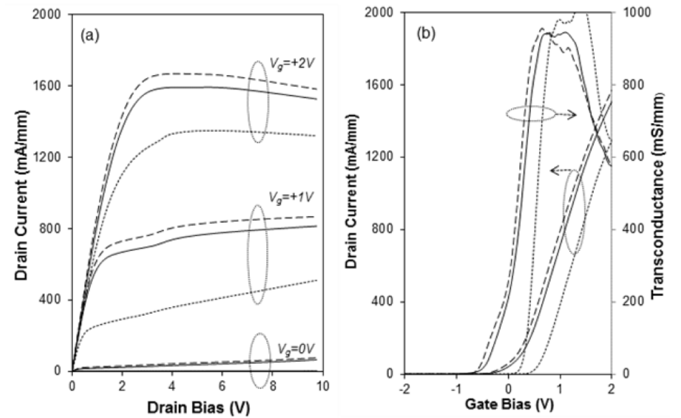

Fig. 2. (a) Output IV characteristics and (b) transfer curves and transconductance for recessed 0.1-μm InAlN/GaN HEMTs fabricated on Wafers A (dotted lines), B (solid lines), and C (dashed lines). The gate bias for the top curve of the IV characteristics is 2 V and the step of the gate bias is -1 V for all the three devices. The transfer curves and transconductances were measured at a V_{ds} of 10 V.

mS/mm, which are within a range of approximately 3%, have been achieved for the Al_2O_3-passivated and SiN-passivated devices on Wafers A, B, and C, respectively, at a V_{ds} of 10 V.

A comparison of the transfer characteristics of the unrecessed Al_2O_3- and SiN-passivated devices at different drain biases indicates that these two passivation technologies hardly change their scaling behaviors. For example, devices on Wafers A and B display not only a similarly small V_{po} shift of about 340 and 330 mV when V_{ds} is increased from 2 to 10 V, but also a similarly low subthreshold swing of 111 and 94 mV/decade at $V_{ds} = 2$ V and 122 and 102 mV/decade at $V_{ds} = 10$ V, as well as a similarly low drain-induced barrier lowering of 60 and 52 mV/V at $V_{ds} = 4$ V and 42 and 43 mV/V at $V_{ds} = 10$ V, respectively.

In Fig. 2, the recessed devices on Wafers B and C show a very similar I_{max} of about 1.6 A/mm at $V_{gs} = 2$ V and $V_{ds} = 10$ V and g_{max} of about 940 S/mm. Wafer A, however, shows a 20% lower I_{max}, primarily due to its deeper etching

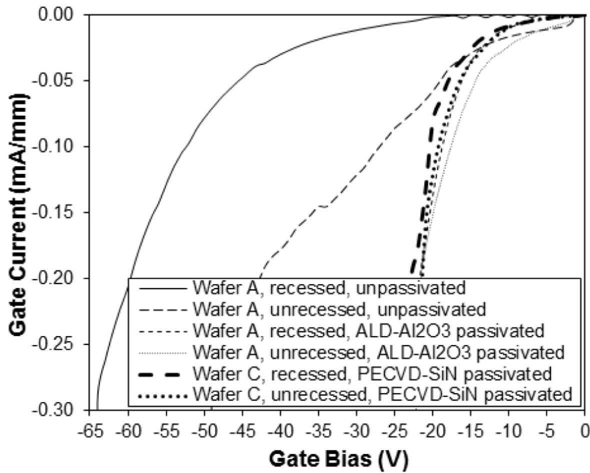

Fig. 3. Reverse Schottky characteristics for unrecessed and recessed 0.1-μm InAlN/GaN HEMTs on Wafer A (both before and after ALD Al_2O_3 passivation), as well as unrecessed and recessed 0.1-μm InAlN/GaN HEMTs on Wafer C after PECVD SiN passivation.

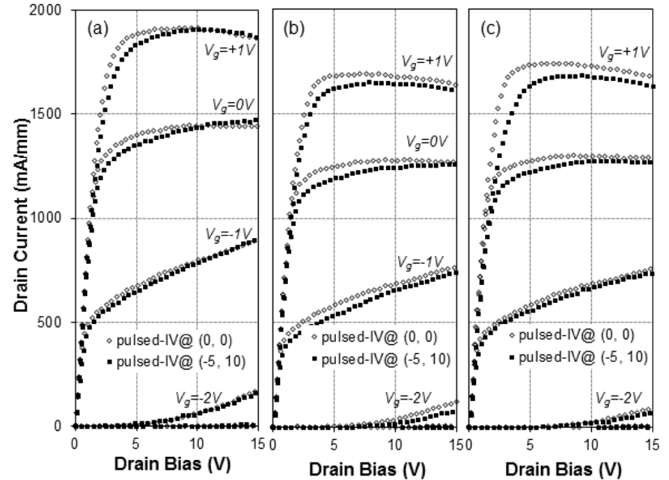

Fig. 4. Pulsed-IV characteristics for unrecessed 0.1-μm InAlN/GaN HEMTs on (a) Wafer A, (b) Wafer B, and (c) Wafer C. The devices were measured at quiescent points of $V_{gs} = 0$ V and $V_{ds} = 0$ V (open symbols) and $V_{gs} = -5$ V and $V_{ds} = 10$ V (solid symbols). The V_{gs} for the top curves is 1 V and the V_{gs} step is -1 V for all devices. The pulsed drain current was measured with 200-ns pulse width and 2-ms separation.

in comparison with the other two wafers. The slightly deeper etching is also largely responsible for the approximate 0.85 V increase in V_{po}, correspondingly leading to enhancement-mode devices with g_{max} boosted by about 8% to 1020 mS/mm. It should be noted that the aforementioned approximately 1-nm deeper etching on Wafer A (compared with Wafers B and C) was due to the process variation as it was etched with nominally the same recipe, giving rise to a 2-nm gate-to-channel distance for the recessed devices on this wafer.

B. Breakdown Voltage

In Fig. 3, the unrecessed device of Wafer A typically has an off-state breakdown voltage BV, defined as the gate–drain voltage at which a gate current I_g of 1 mA/mm is reached with the source electrode floating, of about 50 V before passivation. With the gate recess, the device shows a BV slightly over 60 V. This BV increase with lateral recess width is similar to that of GaAs- and InP-based HEMTs, with enhanced BV resulting from an enlarged lateral recess. However, the above relatively high BV of InAlN/GaN HEMTs would largely disappear after the passivation layer is deposited. Furthermore, the devices with SiN passivation (e.g., Wafer C as shown in Fig. 3) actually exhibited a similar degradation in BV after the passivation, essentially coinciding with their Al_2O_3-passivated counterparts; this is attributed to the conduction path at the interface between the InAlN surface and the passivation layers. It can also be noted that the recessed Al_2O_3-passivated device displays several volts higher BV than the unrecessed one. This small difference between the recessed and unrecessed devices also holds true for their SiN-passivated counterparts on Wafer B, indicating the contribution of lateral recess to higher BV.

It is apparent that there is a need to enhance the breakdown voltage of the InAlN/GaN HEMTs so that they can deliver higher output power at a higher bias or operate more reliably. The most straightforward approach is to modify the passivation process including the pretreatment process. However, this can be made complicated because any adjustment to the passivation would have an impact not only on the breakdown but also on pulsed-IV.

C. Pulsed-IV Characteristics

The pulsed-IV characterization was performed with a pulse width of 200 ns and a separation of 2 ms. The unrecessed device on the Al_2O_3-passivated Wafer A in Fig. 4(a) shows pulsed-IV better than its SiN-passivated counterparts on Wafers B in Fig. 4(b) and C in Fig. 4(c) in terms of pulsed drain current level as well as its collapse, in particular at a relatively low V_{ds} ranging from 2.5 to 5 V. For the two SiN-passivated wafers, it can also be noted that the device on Wafer C shows a slightly larger current collapse than Wafer B in the low V_{ds} regime, which can probably be traced back to its thinner passivation layer, as mentioned in Section II.

In addition to the passivation process, the lateral recess width shows a much more pronounced impact on the pulsed than the dc output characteristics. It is quite obvious, as shown in Fig. 5, that the decrease in lateral recess width from Wafers A, to B and C can be clearly reflected on their corresponding increase in the pulsed drain current. While a deeper recess etching on Wafer A, though unintentional but distinguishable as mentioned in Section III-A, may not be sufficiently convincing to make this comparison conclusive, a 15% difference in the maximum pulsed drain current between Wafers B and C [markedly larger than the approximately 4% difference in their dc I_{max} at the same bias condition as indicated in Fig. 2(a)] at $V_{gs} = 2$ V and $V_{ds} = 10$ V should be attributed to their approximate 10% difference in side etching.

Furthermore, the advantage of ALD-Al_2O_3 over PECVD-SiN as a passivation layer can also be observed in recessed devices in Fig. 5. While the devices on Wafers B and C show much higher pulsed drain currents than Wafer A due to their smaller side recess widths and vertical recess depths, their drain current collapse of about

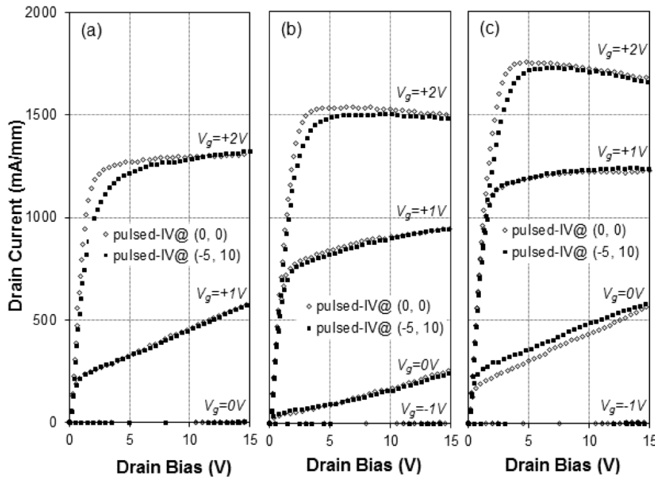

Fig. 5. Pulsed-IV characteristics for recessed 0.1-μm InAlN/GaN HEMTs on (a) Wafer A, (b) Wafer B, and (c) Wafer C. The devices were measured at quiescent points of $V_{gs} = 0$ V and $V_{ds} = 0$ V (open symbols) and $V_{gs} = -5$ V and $V_{ds} = 10$ V (solid symbols). The V_{gs} for the top curves is 2 V and the V_{gs} step is −1 V for all devices. The pulsed drain current was measured with 200-ns pulse width and 2-ms separation.

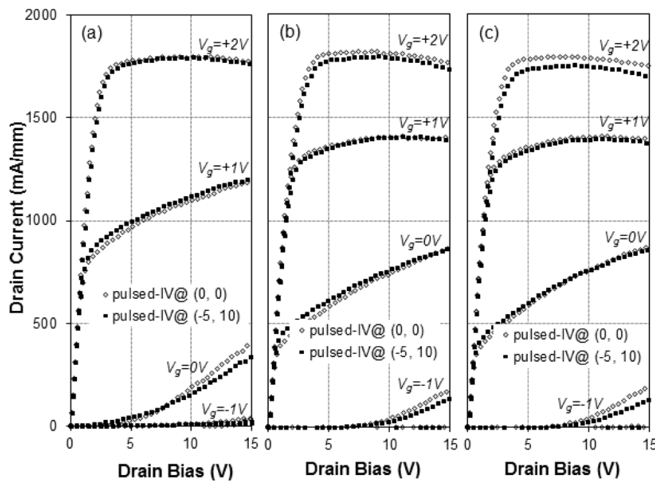

Fig. 6. Pulsed-IV characteristics for 0.1-μm InAlN/GaN HEMTs with only vertical gate recess on (a) Wafer A, (b) Wafer B, and (c) Wafer C. The devices were measured at quiescent points of $V_{gs} = 0$ V and $V_{ds} = 0$ V (open symbols) and $V_{gs} = -5$ V and $V_{ds} = 10$ V (solid symbols). The V_{gs} for the top curves is 2 V and the V_{gs} step is −1 V for all devices. The pulsed drain current was measured with 200-ns pulse width and 2-ms separation.

50 mA/mm at $V_{ds} = 5$ V and 100 mA/mm at $V_{ds} = 2.5$ V, when the quiescent point is switched from $V_{gs} = 0$ V and $V_{ds} = 0$ V to $V_{gs} = -5$ V and $V_{ds} = 10$ V, are not much better than those observed on Wafer A (even with its larger lateral recess), which has been contained to 50 mA/mm at $V_{ds} = 5$ V and 140 mA/mm at $V_{ds} = 2.5$ V.

An unambiguous demonstration of dominant impact of the width of lateral recess of the device on its pulsed-IV characteristics comes from Fig. 6, in which all the three devices with only vertical gate recess show highly similar pulsed drain currents, even though Wafer A actually has a somewhat deeper etching—further evidenced by its V_{po}, shown in Fig. 6(a), which is more positive than those of Wafers B and C. The above observation can be simply explained by the fact that the devices in Fig. 6 all have the same lateral recess width (of zero) as they are only vertically recessed. Clearly as a result, it is the lateral recess width, rather than the vertical recess depth, that is the leading factor in determining the pulsed-IV characteristics. It would be even more revealing to compare the devices in Fig. 6 with their counterparts with lateral recess in Fig. 5: All devices in Fig. 6 without lateral recess have higher pulsed drain currents than their recessed counterparts in Fig. 5 to a varied degree depending on the lateral recess width, no matter how deep the gate recess is.

Not surprisingly, a more careful examination of the pulsed-IV shown in Fig. 6 further discloses that Wafer A has the smallest collapse in pulsed drain current, which further indicates that a better passivation is offered by the ALD Al_2O_3 film. In addition, Wafer C has shown a larger pulsed drain current collapse than Wafer B, which probably could be attributed, at least in part, to its thinner SiN passivation layer, similar to the unrecessed FET on Wafer C shown in Fig. 4(c).

Finally, it is also interesting to notice that V_{po} can also be affected by the gate recess width if one compares devices in Fig. 5 and their counterparts in Fig. 6. It should be noted that the recessed devices with different lateral widths on the same wafer were recessed in the same etching run. Furthermore, the etching process was designed to be performed in self-limiting cycles so that the variation in depths of recess grooves due to either sizes or locations would be minimized. As a result, good uniformity in the recess depth can be achieved, leading to V_{po} standard deviations typically smaller than 150 mV across 4-in wafers for devices with the same topology. Therefore, the V_{po} difference of approximately 0.7 V between the corresponding pairs of devices in Figs. 5 and 6 cannot be fully explained only with the variation in the recess depth as one would intuitively do at the first glimpse; we would attribute the above observed V_{po} difference, at least in part, to the difference in recess width. Similar phenomena were actually reported in InAlAs/InGaAs HEMTs previously [16], [17], which was attributed to the interface traps affecting the sheet carrier density in the channel. In GaN HEMTs, traps are both higher in density and closer to the channel when not passivated properly, and thus have a much more significant influence on the density of the 2DEG channel in comparison with HEMTs based on InAlAs/InGaAs or AlGaAs/InGaAs heterojunctions grown on InP or GaAs substrates. The increased parasitic access resistances resulting from both the lowered sheet carrier density and the enlarged width of the lateral recess areas would be likely to reduce the voltage drop that is actually applied to the intrinsic transistor including the gate and its fringing areas, thus contributing to V_{po} values as shown in Fig. 5 more positive than those of their counterparts without lateral recess as shown in Fig. 6.

D. Small-Signal Characteristics

Fig. 7 shows the current and power gains obtained from on-wafer S-parameter measurement on 2×35 μm unrecessed devices on Wafers A, B, and C over the frequency of 0.5–110 GHz when biased at a V_{ds} of 10 V and a drain current of 500 mA/mm. All the three HEMTs show a similar current gain cutoff frequency of about 100 GHz and a maximum

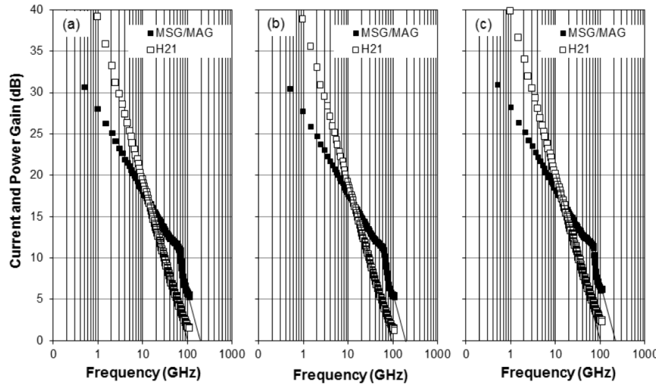

Fig. 7. Current gain and power gain over 0.5–110 GHz for unrecessed 0.1-μm InAlN/GaN HEMTs on (a) Wafer A, (b) Wafer B, and (c) Wafer C. The measurement was performed at a V_{ds} of 10 V and a drain current of 500 mA/mm on 2×35 μm devices on all the three wafers.

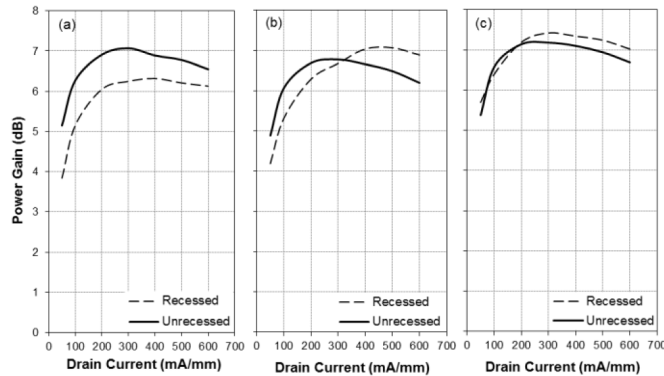

Fig. 8. MAG at 86 GHz as a function of the drain current for unrecessed (solid lines) and recessed (dashed lines) 0.1-μm InAlN/GaN HEMTs on (a) Wafer A, (b) Wafer B, and (c) Wafer C. The measurement was performed at a V_{ds} of 10 V on 2×35 μm devices on all the three wafers.

oscillation frequency of approximately 200 GHz. A more careful examination of the maximum available gain (MAG), however, reveals that Wafers B and C have about 0.3 dB lower and 0.2 dB higher MAG than Wafer A at 86 GHz under the above bias condition, respectively.

To better evaluate the impact of passivation and gate recess on the small-signal power gain, we have plotted the MAG at 86 GHz against the drain current at a fixed $V_{ds} = 10$ V for both the unrecessed (solid line) and recessed devices (dashed lines) on three wafers in Fig. 8(a)–(c). It can be noted that the MAG of both types of devices on Wafer A increases rapidly with the drain current, followed by a gradual drop. The comparison of recessed and unrecessed devices on Wafer A shows that lateral recess of the device does not increase the power gain, completely different from those on Wafers B and C, which do show higher MAG for the recessed devices. It can be noted that the on-resistances extracted from the pulsed-IV biased at $V_{gs} = -5$ V and $V_{ds} = 10$ V for the unrecessed in Fig. 4(a) and recessed devices in Fig. 5(a) on Wafer A are about 1.1 and 1.37 $\Omega \cdot$ mm, essentially in line with the 1.1 and 1.3 $\Omega \cdot$ mm extracted from the dc IV characteristics in Figs. 1(a) and 2(a). The aforementioned lower power gain of the recessed device on Wafer A, when compared with that of the unrecessed on the same wafer, can be attributed to its approximately 20% higher parasitic resistances due to its markedly wider lateral recess, as confirmed by simulation, despite its higher g_m and lower feedback capacitance brought by the gate recess. It is also worth noting that Wafer C displays a distinguishably higher gain in comparison with Wafer B, and that this could be related to its thinner passivation layer.

TABLE I

PERFORMANCE SUMMARY OF REPORTED MMW MMIC PAs AT 71 GHz OR HIGHER [1]–[4] AND THE *E*-BAND MMIC PAs BASED ON THE 0.1-μm InAlN/GaN HEMTs IN THIS WORK. THE BAE SYSTEMS MMIC WAS MEASURED AT $V_{ds} = 10$ V AND $I_{ds} = 500$ mA/mm. THE PERFORMANCE CITED FROM [3] WAS OPTIMIZED FOR HIGH OUTPUT POWER

Ref.	HEMT	# Stages	Freq (GHz)	V_{ds} (V)	Gain Comp (dB)	P_{out} (W)	Pout (W/mm)	PAE (%)	Power Gain (dB)
[1]	0.12µm AlGaN	3	75	35	5	1.3	1.6	6	6
[2]	0.15µm AlGaN	3	88	14	5	0.84	1.4	14.7	9.3
[3]	0.15µm AlGaN	3	91	20	3	1.7	1.53	11	12
[4]	0.14µm AlGaN regrown ohmic	3	93.5	14	5	2.14	1.78	19	11
71-76 GHz Single ended	0.1µm InAlN Unrecessed, ALD Al_2O_3	2	76	10	2.5	0.98	1.75	9.9	4.5
71-76 GHz Balanced	0.1µm InAlN Unrecessed, ALD Al_2O_3	2	76	10	2.2	1.4	1.25	9.7	6.5
81-86 GHz Balanced	0.1µm InAlN Unrecessed, ALD Al_2O_3	2	86	10	1.5	1.43	1.27	12.7	8.5
81-86 GHz Balanced	0.1µm InAlN Unrecessed, PECVD SiN	2	86	10	2.7	1.24	1.11	10.5	7.9
81-86 GHz Balanced	0.1µm InAlN Recessed, PECVD SiN	2	86	10	0.7	1.63	1.46	15.0	9.1

IV. MMIC RESULTS AND DISCUSSION

Several PAs have been designed for optimum output power performance operating at 71–76 and 81–86 GHz with the 0.1-μm InAlN/GaN HEMTs discussed in the previous sections. Their performance has been summarized in Table I and compared with those of the state-of-the-art PAs reported in the past a few years, which are exclusively powered by HEMTs based on AlGaN/GaN heterojunction.

First, the two-stage balanced amplifier based on the unrecessed HEMTs on Wafer A with ALD-Al_2O_3 passivation demonstrates a P_{out} of 1.43 W with an associated PAE of 12.7% at 86 GHz at a 1.5-dB gain compression (where the amplifier is not being driven fully into compression due to limitations of the test setup). This performance is better than the 1.3 W and 6% at 75 GHz of a three-stage PA in [1], comparable to the 0.84 W and 14.7% at 88 GHz of a three-stage PA in [2], as well as the 1.7 W and 11% at 91 GHz of a three-stage PA optimized for high power in [3]; it has lower output power and PAE than that reported in [4], which is a three-stage PA based on 0.14-μm AlGaN/GaN HEMTs with regrown GaN cap for ohmic electrodes with 1-μm spacing.

The performance of this MMIC PA based on unrecessed ALD-Al_2O_3-passivated devices also compares favorably with that of the PA that has the same design and unrecessed devices but with SiN passivation on Wafer C, showing about 15% higher P_{out} (even less compressed by more than 1 dB), more than 2% points higher PAE, and approximately 0.6 dB higher gain. Given the comparable device small-signal equivalent circuits as well as the optimum load impedances for the

above devices with different passivation processes, this MMIC performance comparison can be further interpreted as evidence for the advantage of adopting ALD Al_2O_3 as the passivation layer at the first order.

When the devices were recessed both vertically and laterally, however, the same two-stage E-band amplifier based on SiN passivation devices on Wafer C would show markedly enhanced power performance at 86 GHz. Its P_{out} of 1.63 W and PAE of 15% are not only approximately 30% and 4.5% points higher than the PA based on unrecessed devices on the same wafer, but also 15% and 2.3% points higher than the PA based on ALD-Al_2O_3-passivated unrecessed HEMTs on Wafer A. Probably, this should not be a surprise, given its enhanced gain resulting from the gate recess, as well as the excellent pulsed-IV that is effectively retained due to its relatively narrow lateral recess.

In addition, two PAs operating at 71–76 GHz have also been designed with the 0.1-μm InAlN/GaN HEMTs. Despite limitations of the test setup, the single-ended PA based on unrecessed ALD-Al_2O_3-passivated devices shows a P_{out} of 0.98 W at 76 GHz, which results in a high power density of 1.75 W/mm, essentially attaining the same power density achieved in [4]. The balanced PA version also shows a respectable P_{out} of 1.4 W at 76 GHz. With the expected power performance improvement with a more accurate device model and enhanced breakdown voltage, it can be expected that the InAlN/GaN HEMT would be a very promising device technology for power application at E-band and beyond.

V. Conclusion

We have investigated the impacts of passivation and gate recess on the electrical performance of InAlN/GaN HEMTs, in particular, dc characteristics, pulsed-IV, small signal gains, and the resulting power performance of MMIC PAs at E-band. The ALD-grown Al_2O_3 appears to offer better passivation to the InAlN surface for enhanced power performance than PECVD SiN. However, the latter still offers acceptable passivation for InAlN and turns out to be very competitive when coupled with a properly designed gate recess groove and SiN thickness. The first-pass results of several PAs at 71–76 and 81–86 GHz clearly show the potential of InAlN/GaN HEMT technology for PAs at 71–110 GHz.

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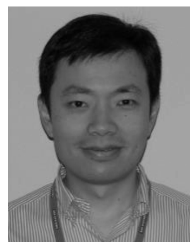
Dong Xu (M'97–SM'07) received the Ph.D. degree from the Walter Schottky Institute, Technical University of Munich, Munich, Germany.

He was with NTT Laboratories, Atsugi, Japan, the University of Notre Dame, Notre Dame, IN, USA, and Global Communication Semiconductors, Torrance, CA, USA, before joining BAE Systems, Nashua, NH, USA, in 2001. His current research interests include millimeter-wave MMICs based on MHEMT and GaN HEMT.



Kanin Chu received the B.S. and Ph.D. degrees in electrical engineering from Cornell University, Ithaca, NY, USA.

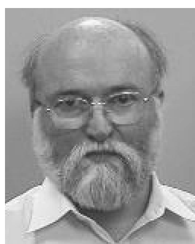
He joined BAE Systems, Nashua, NH, USA, in 2001 to develop advanced MMIC processes based on GaN and GaAs HEMT technologies, where he currently leads the Advanced Processing Group.

Jose A. Diaz received the B.S. degree from the University Interamericana of Puerto Rico, San Juan, Puerto Rico.

He joined Alpha Industries in 1988 as a Production Member in the GaAs wafer foundry. In 2002, he joined the Microelectronics Center, BAE Systems, Nashua, NH, USA.

Michael D. Ashman received the B.S.E.E. degree from the WV Institute of Technology, Montgomery, WV, USA.

He is currently a Senior Principal MMIC Design Engineer with BAE Systems, Nashua, NH, USA, specializing in the development of high-performance microwave and millimeter-wave broadband LNA and PA amplifiers.



J. J. Komiak (M'89–SM'90–F'05) received the Ph.D. degree in electrical engineering from Cornell University, Ithaca, NY, USA, in 1978. His dissertation research developed the Real Frequency Technique for broadband matching an arbitrary load to a resistive generator.

He has 37 years of experience in system, module, and MMIC design for EW, communication, and radar applications. He has over 100 publications and 12 patents.

Louis M. Mt. Pleasant received the B.Sc. degree in electrical engineering from Cornell University, Ithaca, NY, USA.

His current research interests include power and low-noise amplifier monolithic microwave integrated-circuit design, module design, and nonlinear modeling through millimeter-wave frequencies.

Alice Vera received the bachelor's degree in biology form Fitchburg State College, Fitchburg, MA, USA, in 1976.

She has more than 30 years of experience in the development and production of bulk crystals and various epitaxial growth types, characterization, and processing. She is currently a Senior Principal Semiconductor Engineer with the Material and Lithography Group, Microelectronics Center, BAE Systems, Nashua, NH, USA.

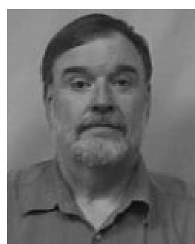
Philip Seekell received the B.S.E.E. degree from the University of Massachusetts, Lowell, MA, USA.

He is currently a Senior Principal Semiconductor Process Engineer with the Photolithography Group, Microelectronic Center, BAE System, Nashua, NH, USA, where he is responsible for e-beam lithography, photolithography, and SEM metrology processes.

Xiaoping Yang received the Ph.D. degree in electrical engineering from Columbia University, New York, NY, USA, in 2001.

He has been with BAE Systems, Nashua, NH, USA, since 2002, where he has been involved in the development of materials for applications from 1 to over 200 GHz. He is currently the Manager with the Material and MMIC Foundry.

Carlton Creamer is a Technology Development Manager with BAE Systems, Nashua, NH, USA, focused on exploiting the company's GaN and GaAs compound semiconductor capabilities for insertion into current and future military electronic systems.



K. B. Nichols received the D.Sc. degree in electrical engineering from Washington University in St. Louis, St. Louis, MO, USA, in 1980.

He is a Program Engineering Manager with the Microelectronics Center, BAE Systems, Nashua, NH, USA, having responsibility for managing program budgets and schedules along with reliability testing and IR thermal analysis.

K. H. George Duh (M'81–SM'13) received the Ph.D. degree in electrical engineering from the University of Minnesota, Minneapolis, MN, USA.

He is currently with BAE Systems, Nashua, NH, USA, where he manages the MMIC and module design activities involved in development of device, circuit, and module technology for microwave and millimeter-wave applications.

Phillip M. Smith (S'80–M'81–SM'88–F'05) received the Ph.D. degree in electrical engineering from Cornell University, Ithaca, NY, USA.

He is currently a Chief Engineer of Advanced Microwave Products with the Systems Microelectronics Center, BAE Systems, Nashua, NH, USA.

P. C. Chao (M'79–SM'88–F'08) received the Ph.D. degree in electrical engineering from Cornell University, Ithaca, NY, USA.

He was the Technical Director of the Microelectronics Center with BAE Systems, Nashua, NH, USA, having responsibility of managing groups in advanced HEMT MMIC processing and reliability testing.

Lin Dong received the Ph.D. degree in electrical engineering from Purdue University, West Lafayette, IN, USA.

He joined the Transistor Technology Group, Applied Materials Inc., Santa Clara, CA, USA, in 2013, where he is currently involved in solving the logic roadmap high value problems through Applied's equipment capability for advanced CMOS technologies.

Peide D. Ye received the Ph.D. degree from the Max-Planck-Institute of Solid State Research, Stuttgart, Germany, in 1996.

He was with NTT, NHMFL/Princeton University, and Bell Labs/Agere Systems, Murray Hill, NJ, USA. He is a Professor of Electrical and Computer Engineering with Purdue University, West Lafayette, IN, USA. His current research interests include ALD high-k integration on novel channel materials.