Analysis of Electron Mobility in Inversion-Mode $Al_2O_3/In_xGa_{1-x}As$ MOSFETs

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***Abstract*—The electron mobility in $Al_2O_3/In_xGa_{1-x}As$ ($x = 0.53$, 0.65, or 0.75) metal–oxide–semiconductor field-effect transistors was analyzed for scattering by oxide charge, as well as interface charge and roughness, and compared with measured transfer characteristics from depletion to inversion. The analysis showed that, under strong inversion, the electron mobility was mainly limited by interface roughness. The extracted interface roughness from the measured data was two to seven times that of the interface between a high-k dielectric and Si, assuming the correlation lengths were comparable. Therefore, to fully benefit from the high bulk mobility of InGaAs, its interface roughness with the gate oxide needs to be further improved.**

***Index Terms*—Charge-carrier mobility, gallium compounds, indium compounds, metal–oxide–semiconductor field-effect transistors (MOSFETs), semiconductor device modeling.**

I. Introduction

THE SUCCESS OF complementary metal–oxide–semiconductor technology is largely based on relentless shrinking of metal–oxide–semiconductor field-effect transistors (MOSFETs) according to Moore's law. As the shrinkage approaches the physical limit of silicon, alternative channel materials such as high-mobility III–V semiconductors have received increasing attention. However, high bulk mobility does not necessarily lead to high surface mobility in an inversion-mode MOSFET. With the recent mapping of interface traps across the bandgap of InGaAs [1] and demonstration of high-performance InGaAs MOSFETs [2]–[15], their current–voltage characteristics can now be analyzed to determine the difference between surface and bulk mobility. This should complement studies that were based on the capacitance–voltage characteristics of metal–oxide–semiconductor diodes and generate new insight into the operation of III–V MOSFETs.

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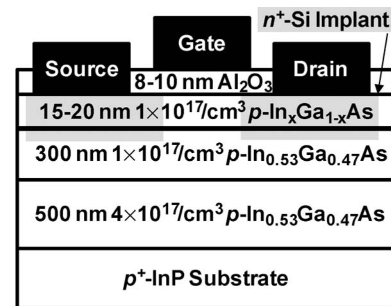

Fig. 1. Schematic cross section of the present InGaAs MOSFETs.

II. Device Structure and Characterization

Fig. 1 illustrates the structure of $In_xGa_{1-x}As$ MOSFETs used in this paper. A 500-nm layer of $In_{0.53}Ga_{0.47}As$ p-doped to 4×10^{17} cm^{-3}, a 300-nm layer of $In_{0.53}Ga_{0.47}As$ p-doped to 1×10^{17} cm^{-3}, and a 15- to 20-nm layer of $In_xGa_{1-x}As$ ($x = 0.53$, 0.65, or 0.75) p-doped to 1×10^{17} cm^{-3} were sequentially grown on p^+-doped InP substrates by molecular beam epitaxy. The $In_{0.53}Ga_{0.47}As$ layer is lattice matched to InP, whereas the $In_{0.75}Ga_{0.25}As$ layer is at the limit of pseudomorphic growth. An 8- to 10-nm layer of Al_2O_3 with a dielectric constant k_{OX} of 9 was then formed on top of $In_xGa_{1-x}As$ by atomic layer deposition as the gate oxide. The gate was metalized with evaporated Ni and Au. Except for the extraction of source–drain parasitic resistance, current–voltage transfer characteristics were measured under a drain–source voltage V_{DS} of 50 mV on MOSFETs with a gate length L of 4 μm and a gate width W of 100 μm. The low drain–source voltage ensured linear characteristics; the long gate length minimized short-channel effects. Several MOSFETs of the same In mole fraction were measured, and the typical characteristics are shown in Fig. 2. It can be seen that, with increasing In mole fraction, the ON-state current and transconductance improve, but the OFF-state leakage degrades. Detailed fabrication process and device performance can be found in [9]. All measurements were performed on-wafer by using an Agilent 4156C precision semiconductor parameter analyzer and a Cascade Summit 12000 probe station with a microchamber ambient enclosure and ± 0.1 °C temperature control.

III. Analysis of Inversion Charge

Despite the high performance of the present InGaAs MOSFETs, their interface trap density is rather high (as will be shown later), and their inversion charge density cannot be

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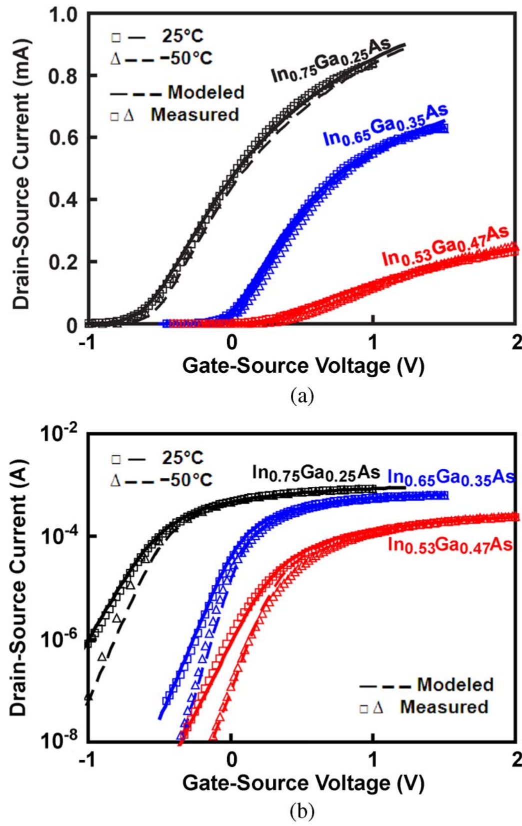


Fig. 2. Excellent agreement in both (a) linear and (b) log scales between (symbols) measured and (curves) modeled transfer characteristics of InGaAs MOSFETs at room temperature and −50 °C. Gate length = 4 μm. Gate width = 100 μm.

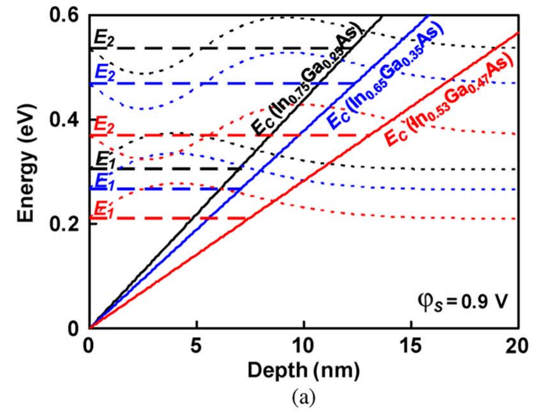
accurately measured. Therefore, instead of extracting from the measured current–voltage characteristics the electron mobility as a function of the inversion charge density, we derive the mobility versus charge density characteristics and reduce them to a few simple parameters to be extracted from the measured current–voltage characteristics, as detailed in this section.

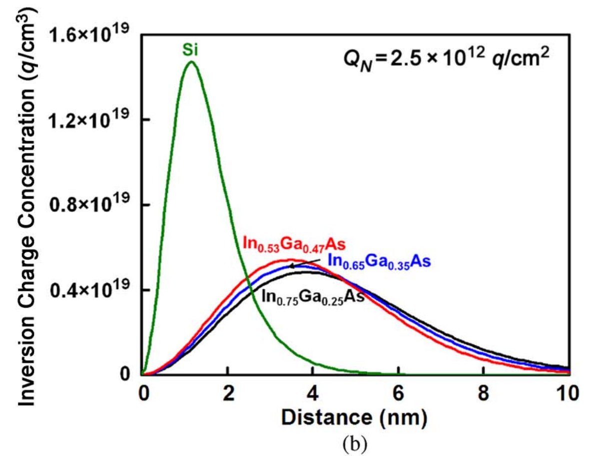
The electrostatic characteristics of the 2-D electron gas in a MOSFET inversion layer can be described by the following coupled Schrödinger and Poisson equations:

$$d^2\psi_I(z)/dz^2 + (2m^*/\hbar^2)\left[E_I + q\varphi(z)\right]\psi_I(z) = 0 \quad (1)$$

$$d^2\varphi(z)/dz^2 = -(q/\varepsilon_s)\left[N_A + n(z) - p(z)\right] \quad (2)$$

where $\psi_I(z)$ is the normalized wave function of an electron in the Ith subband, m^* is the effective mass for the electron motion in the z-direction perpendicular to the oxide–semiconductor interface, $\hbar$ is the reduced Planck's constant, E_I is the energy level of the Ith subband, q is the electron charge, $\varphi(z)$ is the electrostatic potential, ε_S is the semiconductor permittivity, N_A is the ionized acceptor concentration, and $n(z)$ and $p(z)$ are the electron and hole concentrations, respectively. Equations (1) and (2) can be individually but consistently solved by assuming the electric field to be constant or the potential well to be triangular near the interface [16]. For the present InGaAs MOSFETs, Fig. 3(a) shows the lowest two subbands, i.e., E_1 and E_2, and their associated wave functions in the Γ valley under strong inversion. (In the range of inversion charge density explored in this paper, the occupation of satellite valleys is negligible [17].) Fig. 3(b) shows the depth distribution of charge densities summed over all subbands under strong inversion. Fig. 3(c) shows inversion charge density Q_N as a function of surface potential φ_S, which is the potential on the semiconductor surface with respect to that in the semiconductor bulk. For comparison, the calculated charge densities of a silicon MOSFET with $N_A = 1 \times 10^{17}$ cm^{-3} and a 10-nm Al_2O_3 gate oxide are also included. It can be seen that, under strong inversion, the Si MOSFET has a higher charge density than the InGaAs MOSFETs mainly due to a higher density of states in the conduction band. Table I lists the parameter values [18] used in the calculation.





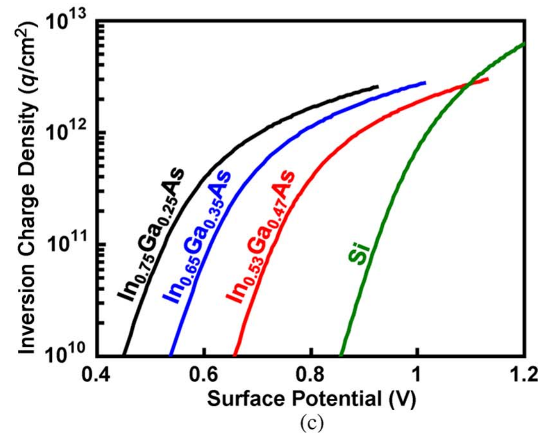


Fig. 3. Calculated (a) wave functions ψ_I, (b) depth distributions, and (c) sheet densities Q_N of the inversion charge in InGaAs MOSFETs. The calculated densities of a Si MOSFET, as listed in Table I, are included for comparison.

TABLE I
MODEL PARAMETERS

Channel	Si	$In_{0.53}Ga_{0.47}As$	$In_{0.65}Ga_{0.35}As$	$In_{0.75}Ga_{0.25}As$
φ_M (V)		5.1		
k_{OX}		9.0		
C_{OX} (F/cm^2)	0.8×10^{-6}	1.0×10^{-6}	0.8×10^{-6}	
k_S[a]	11.7	13.9	14.2	14.4
m^* (m_0[b])	m_T[c] = 0.19 m_L[d] = 0.98	0.041	0.036	0.032
χ (V)	4.05	4.51	4.61	4.69
E_G (eV)	1.12	0.74	0.62	0.53
$E_0 - E_C$ (eV)	−0.50	−0.24	−0.12	−0.04
$E_{F0} - E_C$ (eV)	−0.99	−0.63	−0.51	−0.42
Q_T (q/cm^2)	—	7.4×10^{12}	5.0×10^{12}	7.7×10^{12}
φ_{MS} (V)	0.06	−0.04	−0.02	−0.02
R_{DS} (Ω)	—	14	29	19
μ'_0 (cm^{2}V^{-1}s^{-1})	8.0×10^2	6.5×10^3	8.3×10^3	1.1×10^4
μ_0 (cm^{2}V^{-1}s^{-1})	—	1.3×10^3	1.1×10^4	1.3×10^4
λ/Δ^2 (nm^{-1})	4-63	0.2	0.6	0.7
$\overline{D_{IT}}$ (cm^{-2}eV^{-1})	4.0×10^{11}	1.0×10^{13}	5.7×10^{12}	1.1×10^{13}

[a]relative permittivity of semiconductor [b]electron rest mass
[c]electron transverse mass [d]electron longitudinal mass

Gate–source voltage V_{GS} is related to φ_S by

$$V_{GS} = \varphi_{MS} + \varphi_S - (Q_B + Q_N + Q_{\text{IT}} + Q_T)/C_{\text{OX}} \quad (3)$$

where φ_{MS} is the difference between gate metal and semiconductor work functions, Q_B is the depletion charge density in the bulk of the semiconductor, Q_{IT} is the interface charge density, Q_T is the bulk oxide charge density assumed to be concentrated near the oxide–semiconductor interface, and C_{OX} is the oxide capacitance. To evaluate V_{GS} according to (3), φ_{MS} was calculated by

$$\varphi_{MS} = \varphi_M - \chi - (E_C - E_{F0})/q \quad (4)$$

where φ_M is the metal work function, χ is the electron affinity, E_C is the conduction band minimum, and E_{F0} is the Fermi level in the semiconductor bulk. These parameter values were also included in Table I. Q_B and Q_N were obtained by solving (1) and (2), as previously described.

To calculate interface charge density Q_{IT}, interface trap density D_{IT} and charge neutral level E_0 [19] are needed. Fig. 4 shows the interface trap density between Al_2O_3 and InGaAs across the bandgap as measured by using the charge-pumping method [1]. It can be seen that, in general, the trap density follows a Gaussian distribution with a peak midgap. Since the trap distribution into the conduction band cannot be directly measured, extrapolation is necessary. However, if extrapolation follows the Gaussian distribution, very few traps will be in the conduction band, and the subthreshold slope of the transfer characteristics will be much steeper than what was measured. For lack of better understanding, the trap density in the conduction band is assumed to be constant ($\overline{D_{\text{IT}}}$) and the same as D_{IT} at E_0, as indicated by the solid lines in Fig. 4. Such $\overline{D_{\text{IT}}}$ fits well with the measured transfer characteristics, as shown in Fig. 2.

Following [19], charge neutral level E_0 is assumed to be constant with respect to the vacuum level, and the interface traps are assumed to be donor-like (neutral when filled) below E_0 and acceptor-like (negative when filled) above E_0. Fig. 5 shows the calculated interface charge density Q_{IT} according to

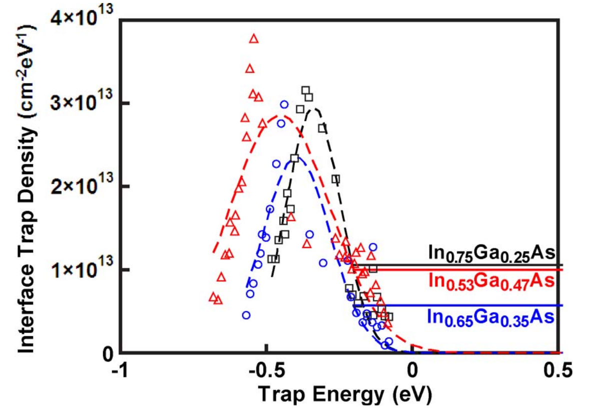


Fig. 4. Interface trap densities D_{IT} in (△) $Al_2O_3/In_{0.53}Ga_{0.47}As$, (○) $In_{0.65}Ga_{0.35}As$, and (□) $In_{0.75}Ga_{0.25}As$ MOSFETs measured by the charge-pumping method across the bandgap. The trap energy is relative to conduction band minimum E_C. (Dashed curves) Gaussian fit. (Solid lines) $\overline{D_{\text{IT}}}$ levels extrapolated from D_{IT} values at charge neutral levels E_0 into the conduction band.

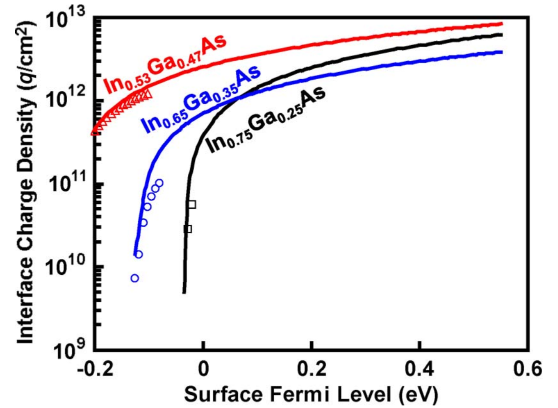


Fig. 5. (Symbols) Measured versus (curves) calculated interface charge densities Q_{IT} for InGaAs MOSFETs.

$$Q_{\text{IT}} = q \int_{E_0}^{E_F} D_{\text{IT}}(E)dE \quad (5)$$

where E_F is the surface Fermi level. The agreement with the experimental data is reasonable.

Fixed oxide charge density Q_T is obtained by fitting the transfer characteristics, as discussed in Section IV. Q_T mainly shifts the current–voltage characteristics along the voltage axis, whereas Q_{IT} also changes its slopes.

IV. ANALYSIS OF ELECTRON MOBILITY

In addition to the inversion charge, low-field electron mobility μ is another important parameter critical to the transfer characteristics of the n-channel MOSFET. Consider the different scattering mechanisms that limit electron mobility, it can be expressed as [20]

$$\frac{1}{\mu} = \frac{1}{\mu_0} + \frac{1}{\mu_R} + \frac{1}{\mu_C} \quad (6)$$

where μ_0 is the semiconductor bulk mobility accounting for the scattering of bulk and remote phonons, as well as ionized impurities, without considering the screening by the inversion charge, μ_R is the interface roughness mobility, and μ_C is the Coulomb scattering mobility due to both oxide charge Q_T and interface charge Q_{IT}.

The InGaAs bulk mobility has been measured in uniform slabs [21] and only needs to be fine-tuned to fit the subthreshold characteristics of the present InGaAs MOSFETs. Table I shows that the measured and fitted values, i.e., μ_0' and μ_0, respectively, are on the same order of magnitude.

In comparison, the interface roughness mobility needs to be derived by calculating the matrix element of the scattering potential before converting to the scattering rate or the relaxation time through the Fermi golden rule. The perturbation potentials for interface roughness scattering V_R [22] and Coulomb scattering V_C [23] are

$$V_R = \frac{1}{4\pi\overline{\varepsilon}} \sum_I \frac{\Delta Q_I}{|\vec{r} - \vec{r_I}|} \tag{7}$$

$$V_C = qE(z)\Delta(x,y) \tag{8}$$

respectively, where ΔQ_I is the charge of the scattering center, $\overline{\varepsilon}$ is the average permittivity, $\vec{r}$ is the position of the electron in the inversion layer, $\vec{r_I}$ is the position of the scattering center, $E(z)$ is the electric field, and $\Delta(x,y)$ is the interface roughness, which is assumed to be Gaussian.

Thus, the interface roughness mobility can be expressed as [23]

$$\mu_R = \left(9\sqrt{\pi}\hbar/4m^* E_{\mathrm{EFF}}\right)\left(\lambda/\Delta^2\right) \tag{9}$$

where λ is the correlation length, Δ is the root-mean-square average of $\Delta(x,y)$, and E_{EFF} is the effective electric field at the interface according to

$$E_{\mathrm{EFF}} = (Q_B + Q_N/2)/\varepsilon_S. \tag{10}$$

Since Q_B and Q_N can be calculated, as shown in Section III, E_{EFF} is known, which leaves λ/Δ^2 as the only fitting parameter for μ_R.

The Coulomb scattering mobility with screening by the inversion charge for the Ith subband can be expressed in (11) [20], shown at the bottom of the page, where

$$\overline{\varepsilon} = (\varepsilon_{\mathrm{OX}} + \varepsilon_S)/2 \tag{12}$$

$$\eta_I = E_I/k_BT \tag{13}$$

$$\overline{z} = -3\left\{\left(12qm^*/\hbar^2\varepsilon_S\right)\left[Q_B + (11/32)Q_N\right]\right\}^{-1/3} \tag{14}$$

$$a = (2/3\hbar)\sqrt{2m^* k_BT} \tag{15}$$

and k_B is Boltzmann's constant. Therefore, according to [20]

$$\mu_C = \sum_I \mu_C(E_I)D(E_I)f(E_I)E_I \Big/ \sum_I D(E_I)f(E_I)E_I \tag{16}$$

where $D(E_I)$ is the density of states in the semiconductor, and $f(E_I)$ is the Fermi–Dirac distribution function. Despite the high interface charge density, the Coulomb scattering mobility in the present InGaAs MOSFETs is calculated to be on the order of 10^4 $\mathrm{cm^2/V/s}$ or higher and, hence, can only affect the total electron mobility under weak inversion. This is probably because, in the present InGaAs MOSFETs, the inverted electrons are farther away from the oxide than those in a Si MOSFET (see Fig. 3). In addition, under strong inversion, the Coulomb scattering is screened by the inversion charge.

As a summary of the aforementioned mobility analysis, Fig. 6 shows the calculated μ_0, μ_R, μ_C, and μ for the present InGaAs MOSFETs at room temperature. It can be seen that, under strong inversion, the total electron mobility decreases with increasing inversion charge and is mainly limited by the interface roughness mobility, as the bulk mobility is rather high in the present InGaAs MOSFETs with $N_A = 1 \times 10^{17}$ $\mathrm{cm^{-3}}$. Even with order-of-magnitude scaling of gate length and doping concentration, the bulk mobility will still be high enough so that, under strong inversion, the total mobility will be mainly limited by interface roughness, unless the interface roughness is significantly improved. By contrast, with higher channel doping and generally lower bulk mobility, the total electron mobility in typical Si MOSFETs is limited by the bulk mobility.

As the interface roughness mobility is not sensitive to temperature, the total electron mobility of the InGaAs MOSFETs exhibits negligible temperature dependence, as shown in Fig. 7. Such temperature insensibility agrees with the experiment data of $In_{0.53}Ga_{0.47}As$ MOSFETs over a much wider temperature range [24]. This confirms that, in the present cases, phonon scattering plays a minor role in determining the electron mobility, particularly when remote phonons are screened by the metal gate [25]–[27].

For compact modeling, the total electron mobility of the present InGaAs MOSFETs under moderate-to-strong inversion can be fitted to a simple power law $E_{\mathrm{EFF}}^{-0.7}$, as shown in Fig. 8. Although it is interesting to extrapolate the power law to 1 MV/cm under which most modern Si MOSFETs operate, it may not be valid because, under such a high field, the electron wave function will move closer to the semiconductor surface and even penetrate into the oxide to degrade the electron mobility faster than what the power law predicts. Unfortunately, high-field tests are not possible because the present InGaAs MOSFETs cannot be biased to higher gate voltages than those shown in Fig. 2. For comparison, the Si universal mobility [28] has also been included in Fig. 8.

$$\mu_C(E_I) = \frac{8\pi\hbar E_I(\overline{\varepsilon}/q)^2}{m^*\left|Q_T + Q_{\mathrm{IT}}\right| \int_0^{\pi/2} \left(1 + a\sqrt{\eta_I}\,\overline{z}\,\sin\varphi\right)^{-6}\left(1 + \frac{q|Q_N|}{6k_BT\overline{\varepsilon}a\sqrt{\eta_I}\,\overline{z}\,\sin\varphi}\right)^{-2} d\varphi} \tag{11}$$

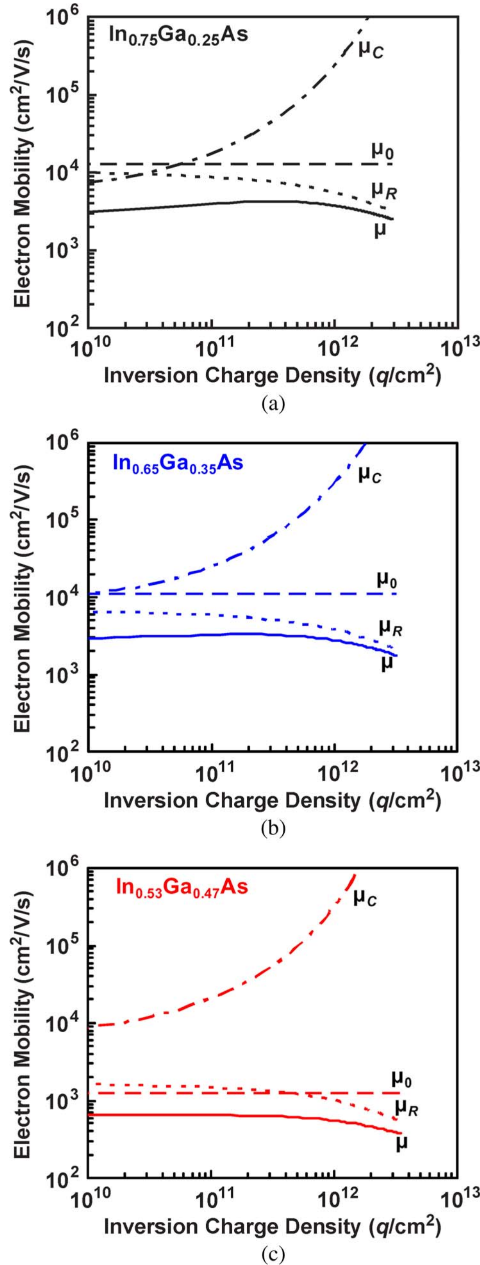


Fig. 6. Calculated semiconductor bulk mobility μ_0 (− − −), interface roughness mobility μ_R (---), Coulomb scattering mobility μ_C(− • −), and total electron mobility μ (——) for (a) $In_{0.75}Ga_{0.25}As$, (b) $In_{0.65}Ga_{0.35}As$, and (c) $In_{0.53}Ga_{0.47}As$ MOSFETs at room temperature. In all cases, μ is mainly limited by μ_R under strong inversion.

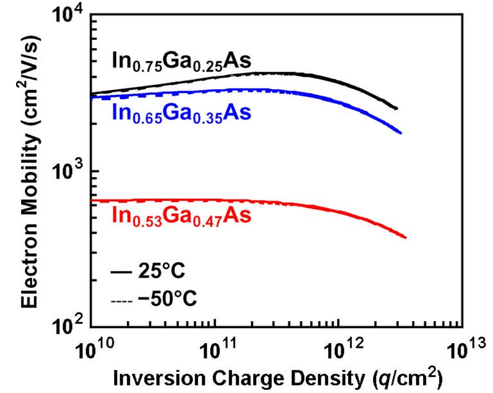


Fig. 7. Total electron mobility μ in InGaAs MOSFETs calculated by using the parameter values listed in Table I, which exhibits little difference between room temperature and −50 °C.

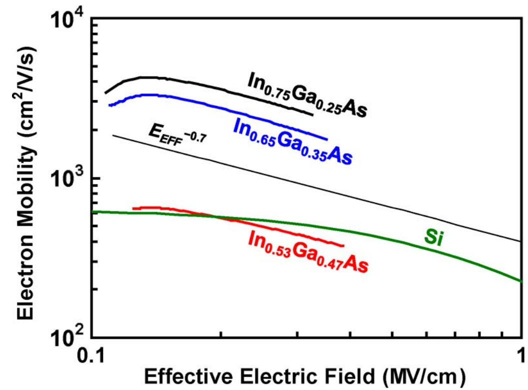


Fig. 8. Total electron mobility μ in InGaAs MOSFETs calculated by using the parameter values listed in Table I, which exhibits simple power-law dependence on effective electric field E_{EFF}. The Si universal mobility [28] has also been included for comparison.

V. Experimental Verification and Discussion

The transfer characteristics can be modeled by

$$I_{DS}(V_{GS}) = \left\{ R_{DS} + \left[\frac{W\mu(V_{GS})Q_N(V_{GS})}{L} \right]^{-1} \right\}^{-1} V_{DS} \tag{17}$$

where I_{DS} is the drain–source current, and R_{DS} is the drain–source series parasitic resistance. The values of R_{DS} were extracted from the measured transfer characteristics of devices with different gate lengths and then optimized to give the best overall fit. Q_N and μ have been calculated in Sections III and IV, respectively, with μ_0 and λ/Δ^2 as fitting parameters. The optimized values were listed in Table I. Fig. 2 compares in both linear and logarithmic scales the modeled and measured transfer characteristics of the present InGaAs MOSFETs with $V_{DS} = 50$ mV at room temperature and −50 °C, respectively. Excellent agreement was achieved from subthreshold to strong inversion.

Table I shows that the extracted interface roughness parameter λ/Δ^2 for the present InGaAs MOSFETs is significantly smaller than that of the Si MOSFET, suggesting that the Al_2O_3/InGaAs interface is rougher than the SiO_2/Si interface. The interface roughness values of Si MOSFETs have been characterized through measurements of carrier mobility [22], [29], [30], atomic force microscopy [31], high-resolution transmission electron microscopy [32], and X-ray reflectivity [33]. For the SiO_2/Si interface, $\lambda = 0.6{-}2.5$ nm and $\Delta = 0.2{-}0.5$ nm. For the interface between a high-k dielectric and Si, λ is usually assumed to be the same, but Δ is slightly larger at 0.3–0.6 nm. Assuming that λ is also the same for the Al_2O_3/InGaAs interface, the extracted λ/Δ^2 implies that $\Delta = 1.2{-}2.2$ nm, which is approximately two to seven times that of the high-k/Si interface. Table I also shows that the interface is significantly rougher when the In mole fraction $x \approx 0.5$, which is consistent with poorer transfer characteristics of the $In_{0.53}Ga_{0.47}As$ MOSFET. However, given the limited sample size, uniformity, and reproducibility, more statistics are needed

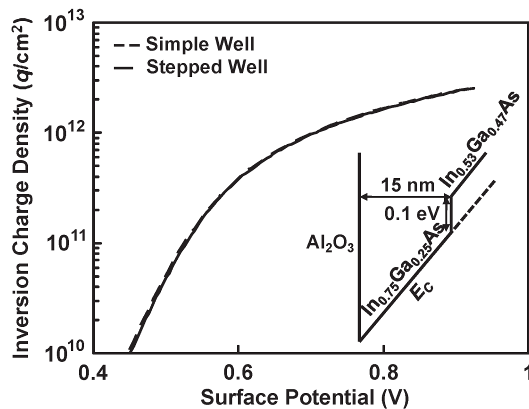


Fig. 9. Calculated inversion charge density Q_N in $In_{0.75}Ga_{0.25}As$ MOSFETs with simple and stepped triangular wells.

before a firm correlation between the interface roughness and the In mole fraction can be established. For the same reason, no firm correlation between interface roughness and interface trap density can be established at the moment. This paper would have been more complete had the interface roughness of InGaAs MOSFETs been characterized through measurements of atomic force microscopy, high-resolution transmission electron microscopy, or X-ray reflectivity as in the case of Si MOSFETs mentioned earlier.

Fig. 4 shows that, for the present InGaAs MOSFETs with high In mole fractions, although the interface trap density is on the order of 10^{13} $cm^{-2}eV^{-1}$ midgap, it rapidly decreases toward the conduction band. Since charge neural level E_0 for high In mole fractions is very close to the conduction band (see Table I), inversion-mode operation with good ON-state performance is achievable, whereas the OFF-state performance is still limited by the high interface trap density below E_0. Furthermore, although the ON-state performance appears to significantly improve with increasing In mole fraction, since the mobility under strong inversion is mainly limited by the interface roughness, the improved ON-state performance cannot be solely attributed to lighter effective mass or higher bulk mobility with increasing In mole fraction. According to (9), the interface roughness mobility is inversely proportional to the effective mass, and the approximately 20% lighter effective mass in $In_{0.75}Ga_{0.25}As$ than that in $In_{0.53}Ga_{0.47}As$ is insufficient to cause the mobility in $In_{0.75}Ga_{0.25}As$ to be approximately three times of that in $In_{0.53}Ga_{0.47}As$. Therefore, the better ON-state performance with increasing In mole fraction of the present InGaAs MOSFETs is mainly due to better interface roughness.

In Section III, the inversion charge was calculated by assuming a simple triangular well (see Fig. 3). In reality, the potential well in $In_{0.65}Ga_{0.35}As$ and $In_{0.75}Ga_{0.25}As$ MOSFETs contains an additional step between the channel and buffer layers, as shown in Fig. 9. However, it is shown in Fig. 9 that the solution of inversion charge density Q_N for the stepped well is very close to that of the triangular well. This validates the approximation by the triangular well.

VI. Conclusion

Unlike in Si MOSFETs, the electron mobility in InGaAs MSOFETs under strong inversion was found to be mainly limited by the interface roughness. By extracting the mobility from the measured transfer characteristics, the roughness of the Al_2O_3/InGaAs interface was determined to be two to seven times of that of the SiO_2/Si interface. Therefore, to fully benefit from the high bulk mobility of InGaAs, its interface roughness with the gate oxide needs to be further improved.

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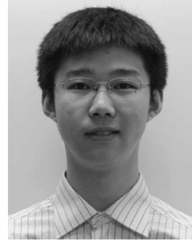

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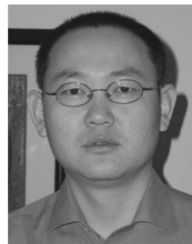

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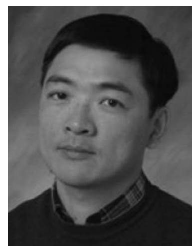

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