# III-V CMOS Devices and Circuits with High-Quality Atomic-Layer-Epitaxial $La_2O_3$/GaAs Interface

L. Dong,[1] X.W. Wang,[2] J.Y. Zhang,[1] X.F. Li,[1] X.B. Lou,[2] N. Conrad,[1] H. Wu,[1] R.G. Gordon,[2] and P. D. Ye[1]

[1] *School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47906, U.S.A.*

[2] *Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA 02138, U.S.A.*

Tel: 1-765-494-7611, Fax: 1-765-496-7443, E-mail: yep@purdue.edu

### *Introduction*

GaAs, as the most studied III-V semiconductor, has been long-time considered to replace Si in logic applications [1]. In order to achieve a thermodynamically stable dielectric on GaAs with a high quality interface, tremendous efforts have been made by different passivation techniques [2-9] since its first publication in 1965 [10]. Recently, we reported high-performance GaAs nMOSFETs with single crystalline La-based oxide dielectrics [11, 12], showing breakthrough in the drive current. In this work, we demonstrate, *for the first time*, high-performance GaAs-based CMOS devices and circuits (inverters, NAND and NOR logic gates, and five-stage ring oscillators). These devices were enabled by the high-quality interface of single-crystalline $La_2O_3$ grown on GaAs(111)A by atomic layer epitaxy (ALE).

### *Experiments*

Fig. 1(a) shows the schematics of nMOSFET and pMOSFET fabricated in this work on a *common* semi-insulating GaAs (111)A substrate with a *common* ALE high-k dielectric. The detailed process flow is depicted in Fig. 1(e). The epitaxial $La_2O_3$ thin films employed here were deposited using lanthanum tris(N,N'-diisopropylformamidinate) and $H_2O$ as precursors at 385 °C, while the amorphous $Al_2O_3$ capping layer was deposited with precursors of trimethylalumnum (TMA) and $H_2O$ at 300 °C. Uniform epitaxial layers were grown by the employment of long purging times (40 s ~ 80 s). The $Al_2O_3$ capping layer is applied to protect the $La_2O_3$ from reacting with the air. The fabricated GaAs MOSFETs in the integrated circuits have a nominal gate length varying from 1 to 8 μm, and the gate width ratios of nMOSFETs to pMOSFETs in GaAs CMOS inverters vary from 1:3 to 1:10. The capacitors were fabricated on p-type GaAs(111)A substrates of doping 5-7×$10^{17}$ $cm^{-3}$ and n-type GaAs(111)A substrates of doping 6-9×$10^{17}$ $cm^{-3}$, with 8nm $La_2O_3$ epitaxial oxide layer and 6 nm $Al_2O_3$ capping layer.

### *Results and Discussion*

Fig. 1(b) shows the atomic structure of the epitaxial $La_2O_3$/GaAs interface. The epitaxial structure of $La_2O_3$ was confirmed by the electron diffraction pattern and HRXRD results (Fig. 1(c)). The coupled 2θ-ω scans suggest that the lattice mismatch of $La_2O_3$ on GaAs(111)A is only 0.04%, if relaxed epitaxy is assumed. A HRTEM image of the epitaxial interface, taken from a sample with 20nm $La_2O_3$ after 860°C annealing, is shown in Fig. 1(d), which further evidences that a flat and sharp interface is formed. A well-behaved output characteristic of a 1μm-gate-length enhancement-mode (E-mode) GaAs(111)A nMOSFET with $La_2O_3$/$Al_2O_3$ is plotted in Fig. 2(a), exhibiting a maximum drain current of 376 mA/mm with $V_{DS}$ = 2 V and $V_{GS}$ = 3.5 V. The transfer characteristics from the same nMOSFET are plotted in Fig. 2(b). A small *SS* of ~74 mV/dec is obtained with an EOT of ~3 nm, indicating a very low mid-gap interface trap density ($D_{it}$) of 2×$10^{11}$ $cm^{-2}$ $eV^{-1}$. The effective electron mobility is depicted in Fig. 2(c) and the peak electron mobility is about 1150 $cm^2$/V·s, which is much higher than the GaAs nMOSFETs with $La_{1.8}Y_{0.2}O_3$ epitaxial dielectric reported previously [11], showing an excellent interface quality enhancement thanks to better crystalline lattice matching [12]. The output and transfer characteristics of E-mode pMOSFETs ($L_{ch}$ = 1 μm) with 780°C and 800°C ion activation annealing are compared in Fig. 3(a-b), respectively. Higher annealing temperature leads to enhanced drain current but also decreased the $I_{ON}/I_{OFF}$ ratio of pMOSFETs (~$10^4$) comparing to nMOSFETs (~$10^7$). It can be ascribed to the heavier Zn dopant diffusion in GaAs under high-temperature. A maximum drain current of 30 mA/mm is obtained for the device annealed at 800°C and a better *SS* of 270 mV/dec is archived in the devices annealed at 780°C. The extracted hole mobility are depicted Fig. 3(c) and the peak hole mobility is about 180 $cm^2$/V·s. Both p-type and n-type high frequency and quasi-static CV characteristics are plotted in Fig. 4(a). The high-frequency CV curves taken from 1kHz to 1MHz show small frequency dispersion at accumulation regions. Surface potentials were determined from the quasi-static CV characteristics using Berglund's equation. The surface potential movement is about 0.94 eV at a gate bias of 1.5 V calculated from p-type CV, while from the n-type CV the surface potential movement is determined to be ~1.06 eV at a gate bias of -2 V. The room temperature conductance method was employed to determine $D_{it}$, which is greatly reduced compared to the amorphous $Al_2O_3$/GaAs(111)A interface, as shown in Fig. 4(b). The temperature-dependent electron effective mobility is shown in Fig. 4(c). The slight increase of the mobility in moderate $N_{inv}$ is due to less phonon scattering while the decreasing mobility at low $N_{inv}$ suggests strong influence of Coulomb scattering. For GaAs based logic circuits, the inverter voltage transfer characteristics are plotted in Fig. 5(a), measured at different supply voltages ($V_{DD}$ = 2, 2.5 and 3 V). The corresponding inverter gain dependences on $V_{in}$ are shown in Fig. 5(b), and a gain of ~12 is obtained with $V_{DD}$ = 3 V. The GaAs CMOS logic circuit operation is further demonstrated by NAND and NOR logic gates. The measured NAND and NOR logic gates outputs are plotted in Fig. 6(a-b), respectively. The supply voltage $V_{DD}$ used in the logic gates is 2.5 V, and for both input and output voltages the logic "1" is corresponding to ~2.5 V while the logic "0" is corresponding to ~0 V (GND). Four combinations of input states "1 1", "0 1", "1 0" and "0 0" and corresponding output results are highlighted. Fig. 7(a) shows a five stage ring oscillator and the corresponding output characteristics. The output power spectrum of the same oscillator is given in Fig. 7(b) and an oscillation frequency of 3.87 MHz is obtained at $V_{DD}$=2.75 V. The fundamental oscillation frequency increases from 0.35 MHz to 3.87 MHz as $V_{DD}$ increases from 1 to 2.75 V.

### *Conclusion*

By realizing a high-quality epitaxial $La_2O_3$/ GaAs(111)A interface, we demonstrate GaAs CMOS devices and integrated circuits including nMOSFETs, pMOSFETs, CMOS inverters, NAND and NOR logic gates and five-stage ring oscillators for the first time. As an exercise of III-V CMOS circuits on a common substrate with a common gate dielectric, it provides a route to realize ultimate high-mobility CMOS on Si if long-time expected breakthroughs of III-V epi-growth on Si occur.

### *References*

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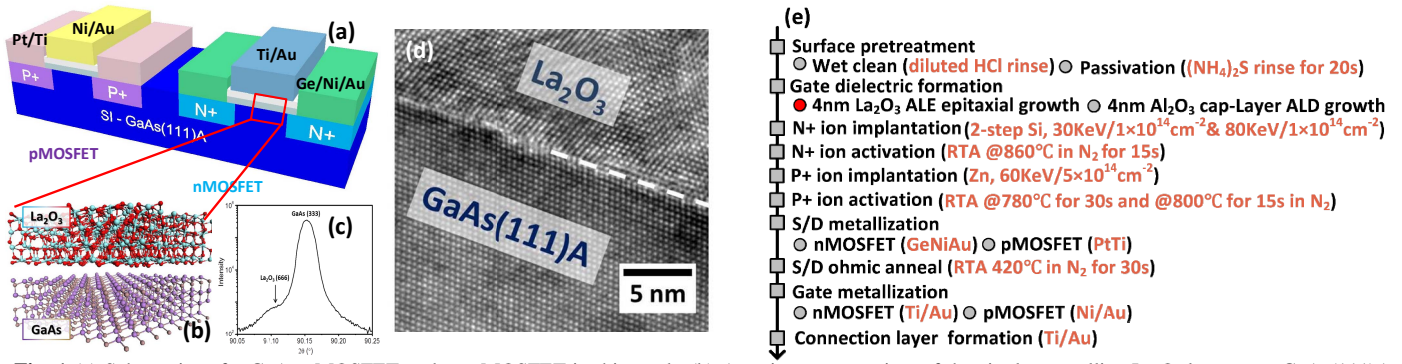


**Fig. 1** (a) Schematics of a GaAs pMOSFET and an nMOSFET in this work. (b) Atomic structure view of the single crystalline $La_2O_3$ layer over GaAs(111)A surface. (c) High-resolution X-ray omega-two theta coupled scan for $La_2O_3$ on GaAs (111)A. The lattice mismatch between the GaAs substrate and the $La_2O_3$ epitaxial film is determined to be ~0.04%. (d) HR-TEM image of a $La_2O_3$/GaAs(111)A epitaxial interface. A flat and sharp interface (denoted by the white dash line) can be observed. (e) Process sequence for the fabrication of GaAs (111)A CMOS circuits. The epitaxial interface is formed by ALE 4nm single crystalline $La_2O_3$, followed by 4nm ALD amorphous $Al_2O_3$ as an encapsulation layer. Si and Zn were used for N+ region and P+ region ion implantation, respectively.

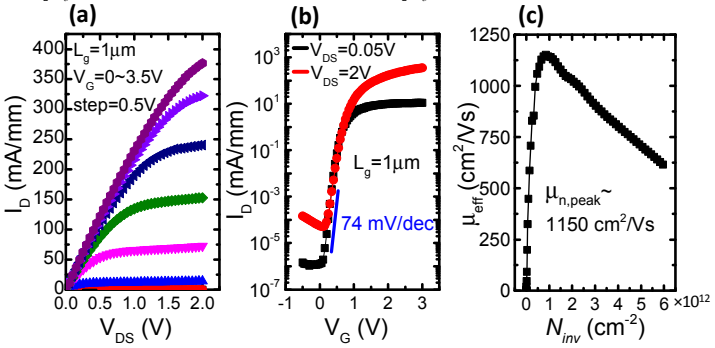


**Fig. 2** (a) Output characteristics for a $L_g$=1μm GaAs(111)A nMOSFET with GaAs/$La_2O_3$ epitaxial interface. (b) Transfer curves of the same device in (a). A low *SS* of 74 mV/dec is obtained. (c) Effective electron mobility extracted from a $L_G$=8μm nMOSFET.

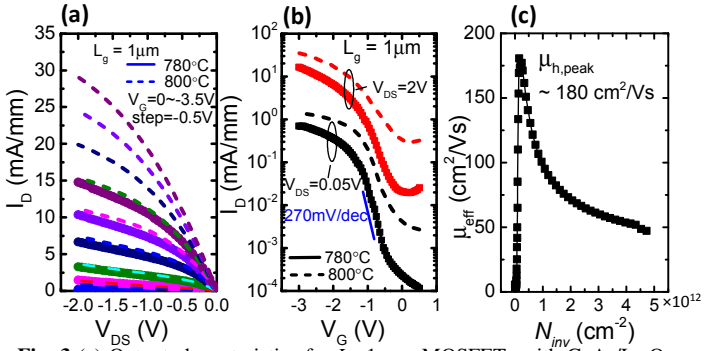


**Fig. 3** (a) Output characteristics for $L_g$=1μm pMOSFETs with GaAs/$La_2O_3$ epitaxial interface annealed at 780°C and 800°C.(b)Transfer curves of the same devices shown in Fig. 6. (c)Effective hole mobility extracted from a $L_G$=8μm pMOSFET annealed at 780°C.

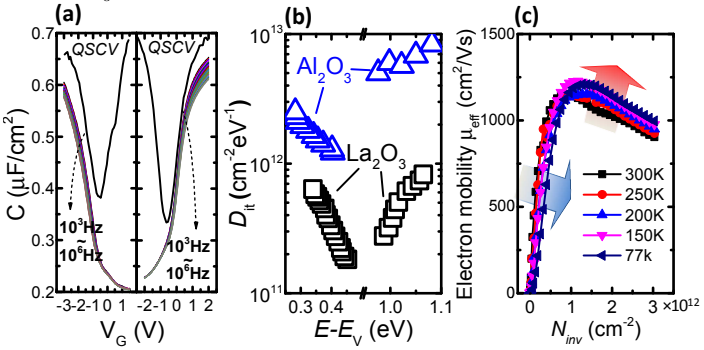


**Fig. 4** (a) Quasistatic and high-frequency C-V cruves of both p-type and n-type capacitors with $La_2O_3$/GaAs epitaxial interface. (b) $D_{it}$ distribution of both amorphous $Al_2O_3$/GaAs(111)A and epitaxial $La_2O_3$/GaAs(111)A interfaces. (c) Electron mobility vs charge density relation in various temperatures.

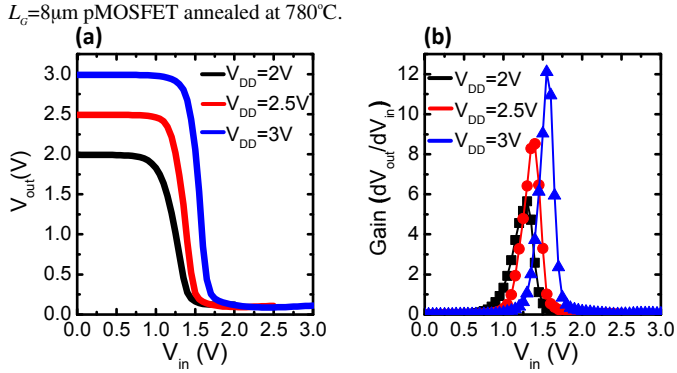


**Fig. 5** (a) Transfer characteristics of a GaAs CMOS inverter, measured with different supply voltages $V_{DD}$ = 2V, 2.5V and 3V. (b) GaAs CMOS inverter gain ($dV_{out}/dV_{in}$) as a function of input voltage. A gain of ~12 is achieved with $V_{DD}$= 3V.

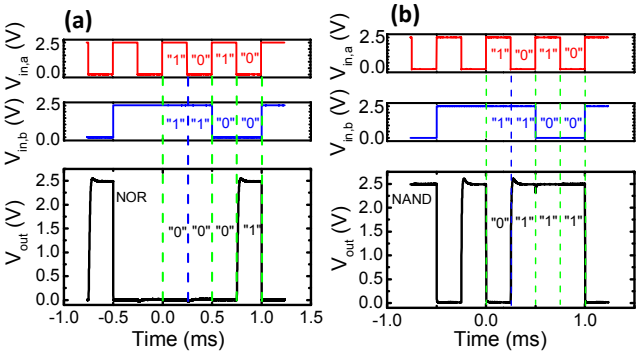


**Fig. 6** (a) $V_{in}$ and $V_{out}$ of the GaAs CMOS NOR logic gate. Four combinations of input states and corresponding output states are marked. (b) $V_{in}$ and $V_{out}$ of the GaAs CMOS NAND logic gate.

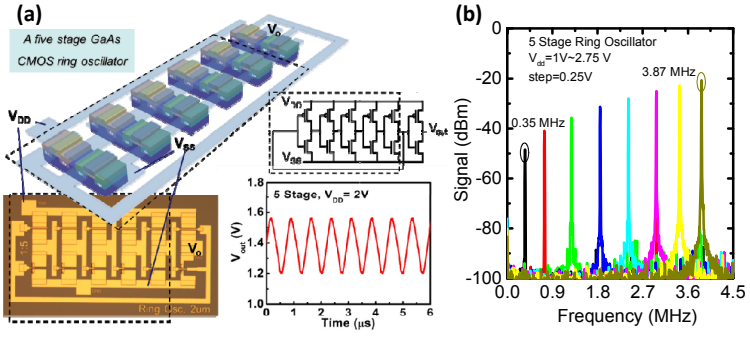


**Fig. 7** (a) Illustration, circuit schematic, optical micrograph and output characteristics of a GaAs CMOS five-stage ring oscillator. (b) Measured output power spectrum of a five-stage GaAs CMOS ring oscillator.